BUSES

FireWire getting hot. IEEE 1394 is the "RCA jack" of tomorrow that will inspire a whole new wave of products and applications. Tom Cantrell, *Computer Design*, 10/97, p. 81, 3 pp.

IC DESIGN

Verification is revolutionizing the IC design process. Shrinking process geometries, increased capacity, and complexity of DSM design set the stage for a new verification methodology. Cheryl Ajluni, *Electronic Design*, 11/3/97, p. 195, 5 pp.

Moving beyond programmable logic. The decision to migrate from PLDs and FPGAs to lower-cost ASICs seems easy at first glance but may be more complicated than you think. Do a little research and analysis before you proceed, and carefully choose which migration path to follow. Brian Dipert, *EDN*, 11/20/97, p. 77, 9 pp.

To create successful designs, know your HDL simulation and synthesis issues. The basis for good Verilog and VHDL designs is a combination of well-structured and efficient simulation and synthesis models with an understanding of simulation and synthesis runtime issues. Douglas J. Smith, *EDN*, 11/6/97, p. 135, 5 pp.

MEMORY

Advanced DRAM architectures overcome data bandwidth limits. Novel architectures for next-generation DRAMs are pushing data-transfer rates beyond 500 MHz while offering new features and control options. Dave Bursky, *Electronic Design*, 11/17/97, p. 73, 9 pp.

MISCELLANEOUS

Focus report: Windows EDA tools. EDA software for Windows NT is moving from point rules to full solutions. Soon, some say, it will win out over Unix. Carolyn Mathas, *Integrated System Design*, 10/97, p. 40, 2 pp.

Mixed-signal methods shift gears for tomorrow's systems-on-a-chip. Standard services still playing key role en route to the single-chip promised land. Charles H. Small, *Computer Design*, 10/97, p. 31, 8 pp.

The voice of the computer is heard in the land (and it listens too!). Computers are starting to do what most two-year-olds can do: identify spoken words and answer back. Richard Comerford, et al, *IEEE Spectrum*, 12/97, p. 39, 9 pp.

PROCESSORS

Compilers for instruction-level parallelism. Discovering and exploiting instruction-level parallelism in code will be key to future increases in microprocessor performance. Michael Schlansker, et al, HP Labs; *Computer*, 12/97, p. 63, 7 pp.

Challenges to combining general-purpose and multimedia processors. Multimedia extensions to general-purpose processors present new challenges to the compiler writer, language designer, and microarchitect. Thomas M. Conte, et al, North Carolina State University; *Computer*, 12/97, p. 33, 4 pp.

Changing interaction of compiler and architecture. Program optimizations that have been exclusively done by either the architecture or the compiler are now being done by both, offering opportunities to optimize performance and redefine the compiler-architecture interface. Sarita V. Adve, et al, Rice University; *Computer*, 12/97, p. 51, 6 pp.

PROGRAMMABLE LOGIC

Years of strong growth lie ahead for high-density programmable devices. Experts agree that programmables have a rosy future, but some say standard cells could make inroads down the line. Larry Waller, *Integrated System Design*, 10/97, p. 28, 4 pp.

High-density FPGA family delivers megagate capacity. Combining blocks of embedded SRAM with up to one million gates, the Virtex family will operate at 150 MHz. Dave Bursky, *Electronic Design*, 11/17/97, p. 67, 3 pp.

SYSTEM DESIGN

KISS those asynchronous-logic problems good-bye. "Keeping It Strictly Synchronous" improves the success rate of digital designs. Steve Knapp, OptiMagic; *Personal Engineering & Instrumentation News*, 11/97, p. 53, 3 pp.

Beaming from here to there—with IR. Support the dawn of the cordless revolution by making the IR port in your portable design shine. The light on the horizon is infrared. Terri Houston, *Portable Design*, 11/97, p. 28, 4 pp.

Distributed power architectures enter the mainstream. Falling component costs and increasing customer performance demands make distributed power the architecture of choice. Lars Thorsell, Ericsson; *Electronic Design*, 11/3/97, p. 127, 5 pp.

Trends in shared-memory multiprocessing. Current application and technology trends are causing researchers and developers to revisit shared-memory multiprocessing. Per Stenstrom, et al, Chalmers University of Technology; *Computer*, 12/97, p. 44, 7 pp.

The system-on-a-chip: It's not just a dream anymore. High-density processes, multiple memory technologies, and mixed-signal capabilities combine to realize what was once unattainable. Dave Bursky, *Electronic Design*, 10/13/97, p. 105, 7 pp.