Hitachi, SGS-Thomson Collaborate on SH-5

Hitachi and European semiconductor maker SGS-Thomson have agreed to combine their 64-bit development efforts and create a jointly owned architecture for embedded systems. Due out in 2001, the new architecture is aimed at "differentiated" products including consumer electronics, games, DVD players, mobile communications, automotive systems, and computer peripherals.

Dubbed SH-5 by Hitachi and ST50 by SGS-Thomson, the new architecture will be completely new but combine aspects of the former's SH-4 family (see MPR 12/29/97, p. 12) with the latter's Chameleon project. The resulting melange will offer backward code compatibility with the SuperH instruction set through some unidentified means, perhaps as a secondary instruction set (à la Merced). The architecture will be 64 bits internally; it seems certain that the compact 16-bit instruction word of the SuperH family will finally give way, perhaps expanding to 32 bits, or to 16 bits with extension words.

Design work for the ST50/SH-5 will be centered in San Jose (Calif.), where both companies have offices. Additional work will come out of SGS-Thomson's Bristol (U.K.) facility and Hitachi's headquarters in Japan. An architectural definition is expected to be complete before the end of 1998, with sample parts in 2000 and production silicon in 2001. Both companies are targeting a 0.18-micron process for the first parts, with clock speeds in the 400-MHz range. Company officers speculated that performance of the new chips would be 500–1,000 MIPS.

The announcement is bittersweet for SGS-Thomson, which had been working on Chameleon, a superscalar 64-bit embedded architecture for image processing. The French company was expected to announce Chameleon in 1998, and early designs were being used within a European multimedia project called Emphasis. Now, the company admits, the ST50 will replace Chameleon. SGS-Thomson cited the difficulties of jump-starting support for a new processor architecture in a market already filled with 32-bit and 64-bit designs.

Hitachi's justification for joining with SGS-Thomson is less clear. Its major apparent benefit is a first-tier alternate supplier with European connections. Both sides confirmed that money is changing hands, but not the amount or the direction. Hitachi is likely to have profited handsomely in the transaction, but for sharing its popular and proprietary processor technology, pecuniary rewards seem uncompelling.

Each company will develop its own products, and the vendors will theoretically compete in the marketplace. Dual-sourcing, which had been a sore spot for both companies, is also an option. Selling or licensing the core is a possibility, although neither company would comment on the likelihood of that possibility. As part of the deal, SGS-Thomson announced it will almost certainly license Hitachi's forthcoming SH-4 family; an option to license SH-3 is likely to remain unexercised.

The new architecture is expected to be 64 bits wide inside and out while remaining compatible with the SuperH instruction set. Simply widening the registers and data paths would permit this; increasing the number of registers, however, would break compatibility. It's possible that the ST50/SH-5 architecture will have more registers than SH-4 does now, but that only some of these would be visible to existing SH binaries. Regarding SuperH's dense instruction encoding, only two opcodes remain undefined. While it's possible that these could be used as "escape hatches" to a new instruction set, it's more likely that SH-5/ST50 will have an entirely new instruction set, with SuperH compatibility provided as a special operating mode. Adding extension words to the base instruction set, as Hitachi did with its SH-DSP core (see MPR 12/4/95, p. 10) is also an option.

Because the SH-5/ST50 architecture is so far away, it's impossible to gauge its impact on the market or its competitiveness against other chip lines. Four years is a long time in this industry, and much can change. What the deal does highlight, however, is the overwhelming lure of the consumer-electronics market and the lengths to which two major companies will go to succeed there. Today, consumer items are fast approaching desktop computers in performance. In the near future, it may be the consumer items that set the pace. —*J.T.*

IBM Matches Motorola Embedded PowerPC

Scant weeks behind Motorola's announcement of low-cost versions of the PowerPC 603e processor (see MPR 10/6/97, p. 8), IBM has followed suit. IBM's EM603e (a slight variation on the Motorola EC603e moniker) is identical to the popular desktop processor in every way except for the absence of a working FPU. Prices of the IBM and Motorola versions are the same for similar speeds grades.

IBM offers the EM603e in 100-, 166-, and 200-MHz speed grades; the company chose not to match Motorola's 133-MHz offering. Announced prices are $20.69, $35.91, and $44.50, respectively, in quantities of 10,000. All three versions are available in a ceramic PGA that is pin-compatible with the desktop 603e processor and thus with several other PowerPC chips. In a small break from the Motorola product line, IBM's 100-MHz part is available in a plastic flat package with an internal heat slug.

With desktop PowerPC prospects looking slim, IBM and Motorola are both focusing renewed effort on placing PowerPC in embedded applications. Specialized embedded chips are certain to come, but in the meantime, these low prices for a slightly crippled 603e will make many embedded designers consider PowerPC more seriously. —*J.T* M