PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,568,646

Multiple instruction-set mapping
Issued: October 22, 1996
Inventor: David V. Jaggar
Assignee: ARM
Filed: September 19, 1994
Claims: 13
A data-processing system with multiple instruction sets. As instructions of a second instruction set pass along the pipeline, they are converted to instructions of the first instruction set. The second instruction set has narrower instructions than the first instruction set and is a subset of it. This allows improved code density but enables one-to-one mapping and avoids a second instruction decoder.

5,568,624

Byte-compare operation for high-performance processor
Issued: October 22, 1996
Inventor: Richard L. Sites, et al
Assignee: Digital
Filed: August 13, 1993
Claims: 19
Byte-manipulation instructions of a RISC instruction set permit use of previously established data structures and include the facility for doing in-register byte extract and insert and masking, along with nonaligned load and store instructions. This patent, one of a series, covers 8-byte general-purpose register (GPR) compare instructions, whereby a packed one-byte result is determined and stored in a GPR, where each bit of the result byte corresponds to the comparison result of two corresponding bytes of the source GPRs.

5,564,118

Past-history filtered branch prediction
Issued: October 8, 1996
Inventor: Simon C. Steely, Jr., et al
Assignee: Digital
Filed: December 8, 1994
Claims: 10
A superscalar, out-of-order, pipelined processor branch-prediction mechanism that maps a stored pattern of histories associated with a branch instruction to a more likely prediction direction of the branch instruction. In one implementation, the branch-prediction mechanism uses two low-order bits XORed with two high-order bits of the target address as an index into the branch-prediction table. The table can store a valid bit and a direction bit or can index prediction counters.

5,564,031

Dynamic allocation of registers to procedures in a digital computer
Issued: October 8, 1996
Inventor: Frederic C. Amerson, et al
Assignee: Hewlett Packard/Hitachi
Filed: April 12, 1996
Claims: 9
In a circular queue, registers in a register file are allocated as temporary local storage for procedures. A called procedure dynamically allocates local registers as needed, without regard to registers used by the caller of the procedure or by any callee of the procedure, whereby register allocation is not restricted by any predetermined window size. Local registers are allocated in the called procedure, rather than at compile time, by adjusting register-stack pointer values. Only the number of registers actually required by the procedure need be allocated. Hardware register-file-access circuitry maps virtual register numbers into the hardware register file. Registers are deallocated by adjusting the register-stack pointers to the values stored when the procedure was called.

5,561,776

Processor architecture supporting multiple speculative branching
Issued: October 1, 1996
Inventor: Valeri Popescu, et al
Assignee: Hyundai
Filed: June 6, 1995
Claims: 55
An out-of-order processor architecture using decoupled instruction fetch and execute. Branch instructions are predicted and results of execution of all instructions are provisionally stored, pending validation or invalidation on the basis of resolving dependencies.

OTHER ISSUED PATENTS

5,566,308 *Processor core that provides a linear extension of an addressable memory space*
5,564,057 *Microprocessor architecture that facilitates input/output utilizing pairs of registers with the same address*
5,564,056 *Method and apparatus for zero extension and bit shifting to preserve register parameters in a microprocessor utilizing register renaming*
5,564,029 *Pipeline processor that avoids resource conflicts*
5,564,028 *Pipelined data processing including instruction trace*
5,564,014 *Apparatus/method for error detecting and retrying individual operands of an instruction*
5,561,782 *Pipelined cache system having low effective latency for nonsequential accesses* M