Motorola May Take ARM License

Sources indicate that processor powerhouse Motorola may have acquired a license to the ARM microprocessor core, to be used in Motorola's telecommunications equipment—cellular telephones and pagers. If so, this would be a political coup for ARM and an indictment of Motorola's own processor architectures.

The ARM architecture has been very successful in the booming wireless telecommunications market because of its static core design, modest power consumption, small die size, and ASIC flexibility. These attributes make it attractive to vendors of digital cellular products that value small size and low power. Several such European and Asian vendors—such as Nokia, Ericsson, and AKM—already use ARM cores. Motorola, which dominates the North American wireless market, is a major exception, choosing to rely on its in-house 6800- and 68000-based processors.

Motorola's dominance has been eroding rapidly as its customers switch from analog to digital wireless services. Last year, Nokia's share of the North American digital wireless market increased threefold and Ericsson's doubled, while Motorola's share plummeted 60%, according to published reports. Much of that shift has been attributed to Motorola's late start and lackluster performance in the digital segment.

By using ARM instead of the 68000, Motorola could presumably increase performance while maintaining low cost and power consumption. ColdFire or PowerPC could offer similar performance, but these processors consume much more space and power than ARM. ARM's Piccolo DSP module *(see* **101504.PDF***)* is also further developed than Motorola's own DSP additions for ColdFire, buying the company important time-to-market advantages. Because of the sensitivity of this arrangement, Motorola may not reveal its ARM licensing plans until later this year, when the first products are available. —*J.T.*

Hitachi SH-DSP Debuts; FP Version in Limbo

The first chip in Hitachi's SH-DSP family has been revealed as the SH7410. An evaluation version of the chip is sampling now, with production slated for 3Q97. The SH-DSP architecture *(see* **091603.PDF***)* integrates a 16-bit fixed-point DSP with the basic SuperH architecture.

Development of Hitachi's SH-3E, on the other hand, seems to have stalled. The planned floating-point unit, announced at the same time as SH-DSP and scheduled to appear in the SH7718 chip late last year, is now in limbo. The SH-3E may never see the light of day, and Hitachi is considering canceling the project in favor of adding FP capability to its audacious SH-4 *(see* **101408.PDF***)*.

The SH7410, built in Hitachi's 0.35-micron CMOS process, will include 48K of ROM, 8K of RAM, and a 32-bit bus interface; the evaluation chip replaces the ROM with more RAM. At 60 MHz, the 3.3-V part will be priced at $25 in 10,000-unit quantities.

Like most vendors of DSP-enabled microprocessors, Hitachi is eyeing the portable cellular market for the 7410. The part should be competitive with Piccolo-based devices from a number of ARM vendors *(see* **101504.PDF***)*. The Hitachi design does not allow the CPU and DSP to execute simultaneously, but it does provide the separate X and Y data memories DSP programmers are used to. Piccolo, on the other hand, can run two instructions at once (within limits) but has to make do with ARM's register set. —*J.T.*

Intel Sues AMD, Cyrix Over MMX Name

Intel has filed suit against AMD and Cyrix in an attempt to restrict how they can use the term MMX to describe their microprocessors. Intel and AMD have been negotiating over this issue for some time, but when AMD issued invitations to a press event announcing the "AMD-K6 MMX processor," Intel had to defend the trademark or risk losing it.

At issue is whether MMX can be protected as a trademark. Intel has filed for a registered trademark, but it has not been granted. Intel has fought for trademarks before: after losing the battle to protect 386, it switched to the Pentium name.

AMD argues that MMX is a generic industry term—an abbreviation for multimedia extensions. It is possible, though difficult, to get a trademark on an abbreviation for a descriptive name. MMX is widely viewed as meaning multimedia extensions, though Intel has said (albeit unconvincingly) that it stands for nothing. AMD says its patent cross-license agreement with Intel *(see* **1001MSB.PDF***)*, as well as numerous Intel statements, describes MMX as meaning multimedia extensions.

The term MMX is widely associated with the Intel-designed instruction-set extensions, and no RISC vendor uses this term to describe similar extensions. Whether Intel did everything it should have to protect the term as a trademark, however, is unclear. AMD asserts that Intel should have chosen a more "fanciful" term, not an abbreviation for a descriptive phrase, to achieve trademark protection.

Having decided it wanted MMX to be a protected trademark, Intel had no choice but to file suit to protect it. The suit is likely to do AMD more good than harm, however, as it has generated a great deal of publicity for AMD's K6 announcement and made it clear that AMD has implemented MMX. Note that this dispute does not concern technology or intellectual property; since it is only a naming battle, it won't affect AMD's ability to ship processors.

The worst-case scenario for AMD is that the company will eventually have to make a slight change in the way it describes the processor, such as using the term "with MMX™ instructions" and crediting the trademark to Intel (in tiny

type at the bottom of the page). AMD might also have to pay some damages, should Intel prevail.

The registered trademark application for MMX is still pending in the United States. Intel has been granted a trademark in Germany, where the law is quite different, and was also granted a preliminary injunction there prohibiting AMD from using the term "AMD-K6 MMX processor" at CeBIT.

Cyrix's M2 is a few months behind the K6 in reaching the market, so the situation with AMD is more pressing. Intel has sued each company separately, but the litigation with AMD should set a precedent for Cyrix and future Intel competitors to follow. —*M.S.*

QED Rolls Out RM52x0 Family

Former design house QED *(see* **1012MSB.PDF***)* has rolled out the first two products to be sold under its own name. Dubbed the RM (for RISCMark) 5230 and 5260, the two chips are identical except for external data-bus width.

The RM5260 is a two-way superscalar device with separate integer and floating-point units, similar to NEC's R4300 and QED's own R5000 designs. The part runs at 150 MHz; the 64-bit external bus runs at a selectable fraction of the core frequency, up to 75 MHz. Dual 16K instruction and data caches are both two-way set-associative, with both write-back and write-through modes supported. As in earlier QED designs, the RM5260 includes a MULADD instruction, for DSP operations, and a special three-operand version of the conventional MIPS multiply instruction. The 5260 fits in a 208-lead package; QED estimates the 150-MHz part consumes 2.8 W from its 3.3-V supply.

The RM5230 is identical to the 5260 but with a 32-bit external bus interface; a smaller, 128-pin package; and a more modest, 2.5-W estimated power budget. The two parts are priced at $35 and $75 in 10,000-piece quantities. Production is set for 3Q97. QED maintains it has already closed deals for both chips but declines to identify its customers.

The new chips are positioned between NEC's R4300 and IDT's R4640/4650. The QED parts offer better floating-point performance than the R4300, because of the NEC chip's longer latencies and lack of a separate FPU. For this improvement, QED charges a modest $10 premium. Compared with the far faster R5000, the QED chips are less expensive due to their smaller caches and lower clock speeds. —*J.T.*

AMD's Elan410 Reduces Cost

AMD beefed up its integrated PC-compatible chip family with the Elan410, a lower-cost version of its existing Elan400 processor *(see* **1014MSB.PDF***)*. Like the 400, the 410 has a 486 CPU core running at 33 or 66 MHz, 8K of unified cache, a 16-bit ISA interface, a DRAM controller, and various PC-compatible peripherals. The 410 eliminates its predecessor's PCMCIA and graphics controllers, which made the 400 more suitable for standalone handheld units.

The two chips are pin-compatible; although the 410 has fewer I/O functions, the two chips share the same 292-contact BGA package. Pricing for the Elan410, which is sampling now, begins at $33 in 10,000-unit quantities.

AMD has received considerable interest in its 486-based Elan400 device since its debut. Intel has no comparable product, offering only the nonintegrated 486GXSF (Hummingbird) and its 386-based 386EX. The larger company has ceded the specialty 486-based market to AMD, which is only too happy to serve. —*J.T.*

Intel/Microsoft NetPC Spec Debuts

Microsoft and Intel have released the NetPC specification, bringing this PC configuration closer to reality. Compaq, Dell, and Hewlett-Packard collaborated in developing the specification. The final document is due to be released in early April, and the first systems should reach the market this summer.

The NetPC is not a network computer (NC) in the Oracle or Sun sense; it is a full Windows PC in which end-user control has been traded off for ease of administration, responding to some of the same issues that prompted the NC but staying within a PC-compatible framework and enabling a range of prices. NetPCs are not expected to be low-cost systems; the cost savings come from reduced cost of ownership, which is generally estimated to be far higher than the actual price of the hardware.

A floppy disk and CD-ROM are optional but not recommended, although the NetPC does require a hard disk. Applications can be booted from a server, but they typically will be run directly from the local disk. To minimize configuration issues, no ISA slots are allowed. PCI slots are for manufacturer or IS department configuration; the box is sealed (locked), and end users cannot add or change cards.

The NetPC specification requires wake-on-LAN capability, which enables the system administrator to remotely manage the system during off hours without keeping the system continuously powered on. ACPI power management is also required. Hardware must be instrumented to allow remote configuration and diagnostics using DMI 2.0.

The CPU must deliver Pentium-133 or better performance; Intel expects systems to use its full range of processors. The minimum memory size is 16M, with 32M recommended. Graphics chips must use either PCI or AGP and provide a minimum resolution of $800 \times 600 \times 16$. USB is required. Physical size is not specified, but systems are likely to be compact.

Intel is developing a related specification, called Wired for Management (WFM), aimed at bringing all of these manageability features to conventional PCs in a consistent way. Such PCs would still have configuration issues, due to the flexibility offered by user-installed options, but they could gain many of the NetPC's benefits. Intel hopes WFM will be more broadly adopted than NetPCs, which it expects will occupy a small market niche.

A NetPC with today's operating systems will provide significant administration benefits, but the full impact won't be felt until Microsoft's Zero Administration Initia-

tive reaches fruition with Windows NT 5.0, due in early 1998. This operating system will allow all user-specific data to be mirrored back to a server, enabling a user to log in at any computer on the network and have access to his or her full environment.

As we go to press, the complete specifications have not been posted; see *www.MDRonline.com/links/PC* for a pointer to the documents as soon as they become available. —*M.S.*

ATI Rage Pro Draws First Blood With AGP

Just one month after announcing the 3D Rage II+DVD, ATI today unveiled its third-generation 3D accelerator family, counting coup over its competitors in several areas. The new 3D Rage Pro is the first chip to support AGP's 133-MHz mode with full use of the pipelining and sideband signals *(see* **100803.PDF***)*; previously announced "AGP-compatible" chips essentially implement 66-MHz PCI instead of the full AGP specification. The ATI part also includes a floating-point 3D setup engine and supports a 100-MHz frame buffer; no previously announced mainstream PC accelerator has either of these features.

The 3D Rage Pro incorporates other features that will be essential for mainstream 3D chips through the remainder of 1997, including support for large frame buffers (up to 8M of SGRAM or 16M of WRAM), a 230-MHz RAMDAC, and MPEG-2 motion compensation. Also included is a 4K cache for 3D textures, which may be stored in local frame-buffer memory or accessed in host memory via the AGP interface.

The 3D setup engine is designed to process up to one million triangles per second, roughly as many as a 266-MHz Pentium II can generate. This match will allow the host CPU to handle 3D geometry and lighting while the graphics chip performs 3D setup, a division generally considered to be the best solution for mass-market 3D through the end of 1997.

The fast frame-buffer interface provides 800 Mbytes/s of peak bandwidth when used with SGRAM. Dual-ported WRAM can yield the equivalent of more than 1.1 Gbytes/s of peak bandwidth, since display refresh overhead does not interfere with normal frame-buffer accesses. These rates are much higher than the bandwidth available from typical PC main-memory subsystems, a difference that will become more pronounced over time as 3D accelerators continue to evolve more quickly than host processors.

ATI (*www.atitech.ca*) says the 3D Rage Pro is sampling now, with production scheduled for June 1997 on UMC's 0.35-micron process. Pricing is set at $30 in 10,000-unit quantities. ATI sells its chips only to motherboard vendors, as it manufactures its own graphics cards. Although several more 3D chips will be introduced over the next few months, none is likely to exceed the performance of ATI's 3D Rage Pro at this cost point. —*P.N.G.* M