PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,561,775

Parallel processing apparatus and method capable of processing plural instructions in parallel or successively
Issued: October 1, 1996
Inventors: Kenichi Kurosawa, et al
Assignee: Hitachi
Filed: December 20, 1994
Claims: 3
A superscalar CPU that includes multiple integer units, a branch unit, and a floating-point unit. The units may process instructions concurrently or, via execution of an instruction, process instructions sequentially. Additionally, an interlock is placed on conditional branch instructions so that, when in parallel-issue mode, no instructions after a conditional branch are issued until the branch has completed.

5,560,028

Software-scheduled superscalar computer architecture
Issued: September 24, 1996
Inventor: Howard G. Sachs, et al
Assignee: Intergraph
Filed: April 13, 1995
Claims: 23
A superscalar computer system whose compiler determines which instructions can be executed in parallel. The system includes a register for storing an arbitrary number of the instructions to be executed. The instructions are tagged with resource tags to identify the resource and to group instructions that may be dispatched simultaneously.

5,560,013

Method of using a target processor to execute programs of a source architecture that uses multiple address spaces
Issued: September 24, 1996
Inventor: Casper A. Scalzi, et al
Assignee: IBM
Filed: December 16, 1994
Claims: 12
A method of utilizing large virtual addressing in a target computer to implement an instruction-set translator for dynamically translating the machine-language instructions of another computer into a set of functionally equivalent target-computer machine-language instructions. The target system provides a unique pointer table in target-virtual-address space that connects each source-program instruction in the multiple source-virtual-address spaces to a target instruction translation that emulates the function of that source instruction in the target system. The target system stores the translated executable source programs by actually storing only one copy of any source program, regardless of the number of source-address spaces in which the source program exists.

5,560,001

Method of operating a processor at a reduced speed
Issued: September 24, 1996
Inventor: James P. Kardach, et al
Assignee: Intel
Filed: September 27, 1995
Claims: 2
A specific implementation and method for controlling the stopping of the clock signal utilized by the Pentium and Pentium Pro CPUs. The patent describes one implementation of STPCLK# by having the processor's microcode engine respond to the external pin. The interrupt mechanism ensures that the processor never has its clock stopped in the middle of a bus cycle.

5,559,976

System for instruction completion independent of result write-back responsive to both exception-free completion of execution and completion of all logically prior instructions
Issued: September 24, 1996
Inventor: Seungyoon P. Song
Assignee: IBM
Filed: March 31, 1994
Claims: 24
A superscalar processing system with multiple execution units employing out-of-order execution. Instructions are retired in order but may retire before instruction results are actually written. Certain instructions, such as STORE and certain register moves, do not use the system's rename buffer but move data directly and therefore must be executed in order. A tag indicates instructions that must be executed in order.

OTHER ISSUED PATENTS

5,560,035 *RISC microprocessor architecture implementing multiple typed register sets*
5,560,032 *High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution*
5,560,017 *System with clock-frequency controller responsive to interrupt independent of software routine and software loop repeatedly executing instruction to slow down system clock*
5,559,974 *Decoder having independently loaded micro-alias and macro-alias registers accessible simultaneously by one micro-operation* M