MOST SIGNIFICANT BITS

PA-8500 Sports 1.5M On-Chip Cache

At the recent CompCon, Hewlett-Packard revealed that its forthcoming PA-8500 processor will include a stunning 1.5M of on-chip cache, five times more than any other announced microprocessor. This unique design, coupled with a significant boost in clock speed, should enable the chip to offer outstanding performance on both SPEC benchmarks and larger applications. The chip has not yet taped out, however, and its production date has slipped into 2H98.

The PA-8500 is based on a 0.25-micron shrink of the PA-8200, which HP builds in an elderly 0.5-micron process. The company has not yet revealed the fab for the PA-8500, but we expect HP to go to an outside foundry due to a lack of competitive process technology internally. Assuming the new chip is built in a true 0.25-micron process such as Intel's P856 or AMD's CS-44 *(see* **101203.PDF***)*, the 8x00 CPU core, currently weighing in at 345 mm^2, would consume only 80 mm^2, according to our estimates.

To take advantage of this shrink, HP could have increased the throughput of the CPU by adding more function units or reorder logic, but these changes would have required significantly more design effort. Instead, the company is making only minor tweaks to the CPU core while wrapping an enormous cache around it. HP did not disclose the PA-8500's die size but noted that the cache consumes three quarters of the die; given our estimate of the core size, we believe the PA 8500 will be about the same size as its predecessors. Essentially, the chip is a 16-Mbit SRAM with one quarter of the die devoted to CPU instead of memory.

The cache is partitioned as 0.5M for instructions and 1M for data, similar to current PA-8000 systems, which use external 1M caches. By moving these primary caches on chip, HP can make them four-way set associative rather than direct mapped, so the hit rate may actually be better than in current systems. With such large caches on chip, no external cache will be necessary. Moving the caches on chip will maintain a fully pipelined cache at higher clock speeds and should also bring the processor's pin count down from over a thousand to a more manageable six hundred or so.

The two-generation process shrink should also greatly increase the clock speed. HP did not release an estimated clock rate, but we believe the PA-8500 could reach 400 MHz, roughly twice the speed of the PA-8200. It would be difficult to get such a large on-chip cache to cycle at that speed, but the 8x00 pipeline already allows two full cycles for cache latency, making the 400-MHz mark more attainable.

This clock speed will be needed to achieve HP's performance goals of more than 30 SPECint95 and 50 SPECfp95 (base). This performance would approach that of Digital's 21264, due to appear in 2Q98 *(see* **110303.PDF***)*. The 21264 will open a big performance lead over HP's chips, but the PA-8500 should put HP back into the performance race. —*L.G.*

Klamath Becomes Pentium II

In a decision that could only have been made by committee, Intel has named its next-generation P6 processor Pentium II. The chip, code-named Klamath *(see* **110201.PDF***)*, is expected to be formally announced in the next few months. Presumably, future P6 derivatives such as Deschutes and Katmai will also carry the Pentium II appellation, much as several generations of the P5 design have been marketed under the Pentium name. One wag joked that the forthcoming Deschutes and Merced should be marketed as Pentium IIB and Pentium NOT IIB, respectively.

Intel takes product branding very seriously; the company has spent hundreds of millions of dollars building the Pentium brand. By selecting the unassuming Pentium II name for its future processors, Intel seeks to leverage this massive investment.

The Pentium name was originally selected to get away from the simple numbering scheme of earlier x86 devices, but the new nomenclature, despite the disguise of Roman notation, merely starts a new numbering sequence. Perhaps future Intel processors, like Super Bowls, will be known only by ponderous Roman numerals. —*L.G.*

Intel Offers P55C-Based Upgrade Chip

Taking advantage of its new P55C processor, Intel is offering a version of the device that upgrades existing Pentium PCs. The new OverDrive product fits into systems using Pentium chips at 75, 90, and 100 MHz. With the OverDrive device installed, the new processor runs at a 66% higher clock speed; for example, a 90-MHz system is upgraded to 150 MHz. The new chip's larger caches and improved pipeline increase application performance by an additional 10%, and its MMX capabilities can improve multimedia software by an even greater amount. Intel expects the new OverDrive processor to deliver a 40–50% performance gain on typical PC applications.

The new product is essentially identical to a standard P55C except for the packaging. Because the OverDrive product must plug into Socket 5 systems that provide only 3.3 V, a voltage regulator is mounted on the PGA package to convert the power input to the 2.8 V needed by the P55C core. The package also sports an integrated fan and heatsink to cool both the CPU and the voltage regulator, which together can dissipate up to 20 W. Like other OverDrive processors, the new chip uses a preconfigured core-to-bus clock ratio that overrides the selections on the motherboard.

A P55C upgrade for a 100-MHz system carries a suggested retail price of $499. A similar chip for upgrading 75- and 90-MHz systems has an SRP of $399. Intel also reduced the SRP of an earlier OverDrive chip, designed to upgrade 60/66-MHz Pentium PCs, to $219. All of these products sell in unit quantities through retail channels.

Intel plans to provide a faster P55C OverDrive processor in 2H97 that will upgrade Pentium-120 and -133 systems to 180 and 200 MHz, respectively. This chip could also be used in faster Pentium systems, but the performance gain would not be as great, and Intel won't promote the product for these systems. A few users with fast Pentium systems may wish to upgrade to gain access to MMX, however.

The company does not plan to offer an upgrade for P55C systems. Such an upgrade would require retrofitting a P6 core into a Pentium pinout; the P24T OverDrive chip, which combined a Pentium core and a 486 pinout, was a huge effort with little return on investment, and Intel isn't willing to repeat this performance. The company plans to deploy a Pentium II OverDrive part to upgrade Pentium Pro systems sometime in 1998, but that may be the end of the OverDrive line. Pentium II systems are likely to be upgraded either by simply replacing the processor daughtercard or by installing a second processor and running MP software. —*L.G.*

IBM Boosts Speed of PowerPC 403 Chips

Improved yields have allowed IBM to boost the speed of two of its PowerPC devices and introduce a new clock-doubled chip. The new 403GCX is similar to the 403GC *(see* **091202.PDF***)* but with much larger caches and higher clock speeds. The 66-MHz 'GCX, now sampling, has 16K of instruction cache and 8K of data cache to support the faster core.

IBM also announced 40-MHz upgrades of the 403GA and 403GC. The 'GA, 'GC, and 'GCX are all pin-compatible; a 25- or 33-MHz system can be upgraded simply by replacing the 403GA or 'GC with a 50- or 66-MHz 'GCX. According to IBM, an 80-MHz 'GCX is probably not in the cards, as its performance might overlap that of the planned 405-series PowerPC core, a higher-performance device due to appear next year. The long-awaited 405 has been due "next year" for the past couple of years, however, so faster 'GCX parts may yet see the light of day.

In 10,000-unit lots, the 403GCX chips are priced at $37 and $45; the new 40-MHz 'GA and 'GC sell for about $23. IBM's embedded PowerPC prices have been consistently lower than Motorola's as the company strives to gain market share and build a reputation for its fledgling CPU business. At only $11, IBM's 50-MHz 401GF *(see* **100802.PDF***)* remains an excellent value for embedded customers. —*J.T.*

StrongARM Gets Core-Logic Support Chip

Trading on its experience with PCI bridge chips, Digital has produced its first support device for its SA-110 StrongArm processor. The new 21285 combines an SDRAM controller, PCI master/slave interface, and ROM port in a 256-contact BGA package. The new chip, due to sample next quarter, will sell for about $20 in quantity.

In its most straightforward configuration, the 21285 can give the SA-110 glueless access to SDRAM and PCI peripherals, replacing custom logic or PLDs. Because the 21285 is also a PCI slave, the chip can be used with an SA-110 to add intelligence to PCI peripheral controllers, *à la* Intel's i960RP and 'RD *(see* **090802.PDF***)*. The 21285 provides I_2O support similar to the i960's, including arbiter, interrupt, DMA, and mailbox/doorbell units. Unlike the Intel devices, the 21285 has no downstream PCI port, but it can supply local intelligence in the form of the SA-110.

The combined price of a $30–$50 SA-110 and a $20 21285 places Digital's solution between the $50 i960RP and the $100 i960RD *(see* **1102MSB.PDF***)*; the two-chip set requires more PCB real estate, however. In Digital's favor, a 233-MHz SA-110 outperforms a 33-MHz i960RP by nearly an order of magnitude while consuming about the same amount of power. Digital expects a combined single-chip version of the SA-110/21285 before long, giving Intel's RISC family a run for its money. —*J.T.*

SDX: Another New Disk Interface

Western Digital's new Storage Data Acceleration (SDX) standard defines a two-bit parallel interface that connects removable-media storage devices—especially CD-ROMs—to SDX-equipped hard-disk drives. The new interface uses a 10-pin cable between the hard disk and CD-ROM drives to create a virtual IDE device said to be completely compatible with existing PC BIOS code, drivers, and software. Since the SDX device appears to be an IDE slave, it will displace any secondary IDE device on the same IDE cable.

Western Digital says SDX will improve the performance of CD-ROMs by transparently caching CD-ROM data on the hard disk. SDX requires OEMs to permanently allocate a significant amount of hard-disk space to this cache, however, and uses a primitive caching algorithm. If 150M of the hard disk is allocated to the cache, for example, only the first 150M of the CD-ROM will be cached.

SDX is even less relevant for DVD. Upcoming 2× and 4× DVD drives will be faster than any CD-ROM drive, and DVD titles will hold much more data than can be cached on common hard disks.

The new interface seems certain, however, to get a chance to prove itself. Many companies—Sanyo, MKE, Toshiba, Panasonic, Teac, and others—have pledged to introduce SDX products. Motorola, SGS-Thomson, and other semiconductor companies have signed on to produce SDX-compatible controller and interface chips. SDX CD-ROM drives should be somewhat less expensive than IDE drives, since functions such as data buffering and error correction can be performed by equivalent logic in the hard-disk drive. These cost reductions may translate into higher margins for makers of CD-ROM drives, certainly an attractive proposition in a highly competitive market.

With the recent UltraDMA/33 upgrade to the IDE interface and the ongoing development of IEEE-1394, SDX seems an inadequate and very temporary addition to the mass-storage market. Compared with existing software-based caches that use system memory and temporary hard-disk buffers, SDX is an inferior solution. —*P.N.G.*