PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,553,276

Self-timed processor with dynamic clock generator having plurality of tracking elements for outputting sequencing signals to functional units
Issued: September 3, 1996
Inventor: Mark E. Dean
Assignee: IBM
Filed: August 31, 1994
Claims: 20
A method and system are provided for self-timed, asynchronous processing. An operation is executed with a function unit. A timing of the operation execution is simulated with a tracking element, and a tracking signal is output. A sequencing signal is varied to the function unit in response to the tracking signal.

5,553,256

Apparatus for pipeline streamlining where resources are immediate or certainly retired
Issued: September 3, 1996
Inventors: Michael A. Fetterman, et al
Assignee: Intel
Filed: June 5, 1995
Claims: 5
Maximum throughput or back-to-back scheduling of dependent instructions in a pipelined processor is achieved by maximizing the efficiency with which the processor determines the availability of the source operands of a dependent instruction through multiple, described mechanisms.

5,553,255

Data processor with programmable levels of speculative instruction fetching and method of operation
Issued: September 3, 1996
Inventors: Danny K. Jain, et al
Assignee: Motorola/IBM
Filed: April 27, 1995
Claims: 6
A data processor with branch-prediction unit that predicts conditional branch instructions and a control unit that monitors the number of unresolved branch instructions. The control unit is allowed to fetch instructions indicated by the branch-prediction unit, depending upon the number of unresolved branch instructions. The number of unresolved branch instructions is user programmable.

5,548,737

Dynamic load balancing for a multiprocessor pipeline by sorting instructions based on predetermined execution time
Issued: August 20, 1996
Inventor: Jimmie D. Edrington, et al
Assignee: IBM
Filed: April 11, 1995
Claims: 28
An apparatus for processing high-level instructions, including multiple processing units, means for generating a plurality of instructions to perform the high-level instructions, and means for dynamically organizing the generated instructions into at least one group, each group including at least one instruction to be processed by one of the processing units. In addition, a method of processing high-level instructions by multiple processing units, including generating multiple instructions to perform the high-level instructions and dynamically organizing those instructions into groups.

5,546,552

Method for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor
Issued: August 13, 1996
Inventors: Brett Coon, et al
Assignee: Seiko Epson
Filed: May 12, 1995
Claims: 7
System and method for extracting complex, variable-length computer instructions, each subdivided into a variable number of instruction bytes, and aligning instruction bytes of instructions. The isolated complex instructions are decoded into nano-instructions that are processed by a RISC processor core.

5,546,545

Rotating priority-selection logic circuit
Issued: August 13, 1996
Inventor: Stephen E. Rich
Assignee: IBM
Filed: December 9, 1994
Claims: 6
A rotating priority-selection circuit selects the oldest instruction with ready operands for execution in a microprocessor that allows for out-of-order execution.

OTHER ISSUED PATENTS

5,548,736 *Method and apparatus overcoming delay introduced by instruction interlocking in pipelined instruction execution*
5,546,599 *Processing system and method of operation for processing dispatched instructions with detected exceptions* M