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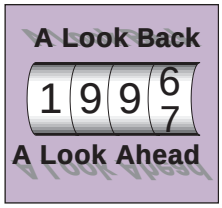
MICROPROCESSOR REPORT

THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

Alpha Sails, PowerPC Flails

x86 Poses Significant Threat to RISC Workstation Sales



by Linley Gwennap

Last issue, we reviewed the x86 market. Our New Year's coverage continues with articles about general-purpose RISC processors, media processors (see page 10), and embedded processors (see page 16).

During the past year, market prospects for PowerPC melted faster than ice cream on an Exponential chip, despite a renewed effort by the processor vendors to deliver competitive price/performance. Apple's problems proved too severe to fix quickly, and the company lost a third of its market share. After finally loosening its hold on Mac OS, Apple failed to find any other significant system maker to boost the Mac platform. The year ended with a whimper when IBM and Motorola admitted that not even their own internal systems groups are interested in Windows NT on PowerPC.

This announcement, combined with strong execution by Digital, puts Alpha in a surprisingly good position. After brief incursions by Intel and HP, Digital regained the microprocessor performance lead last fall, as Figure 1 shows. With the announcement of the 21264, due around the end of this year, Digital set a high hurdle for any vendor wishing to challenge that lead. Perhaps more important, Alpha is now the only RISC architecture supporting Windows NT and thus is the only alternative to x86 in this growing market. The company is pinning its NT hopes on the 21164PC, a new low-cost device due in 2Q97, along with x86 compatibility provided by its FX!32 emulator/translator.

In the meantime, uncharacteristically weak execution let Intel's boot heel slip ever so slightly off the throat of its RISC competition. After dramatically gaining the integer performance lead in late 1995 with its 200-MHz Pentium Pro, the company has yet to announce a faster processor, watching idly as most of the RISC vendors passed Intel's best performance. Worse yet, faster parts such as Klamath, Deschutes, and Merced have reportedly slipped 3–6 months. We still believe that market forces leave Intel well positioned in the workstation and server markets that have been the core of RISC's success, but Intel's slippage gives the RISC vendors a bit more breathing room.

Once again, we offer our RISCie awards to acknowledge the best and worst RISC events of 1996. This year, we decided to let Intel join in the fun as an honorary RISC vendor. For the purposes of these awards, however, we have left out other x86 processor vendors as well as RISC processors aimed at the embedded market.

Digital Bets on NT

Another year, another title. Digital grabs its fourth award for **World's Fastest Microprocessor (shipping)**, this time for the 500-MHz 21164, rated at 12.6 SPECint95 (base). Yields on this chip seem to be good, so we expect Digital to squeeze out a speed boost, perhaps to 550 MHz, in the next few months. The company has demonstrated 600-MHz parts, but this frequency may not be attainable in volume production.

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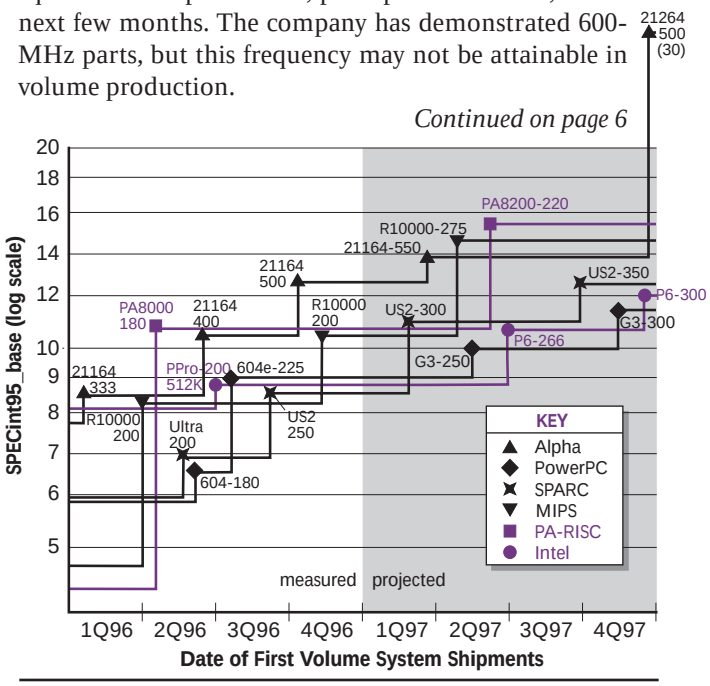

Figure 1. Digital will see increased competition for the integer performance lead in 1997, but the 21264 will be its trump card. (Source: SPEC for 1996 data, MDR for 1997)

AT A GLANCE

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■ THE EDITORIAL VIEW

What's NeXT for Apple?

New OS Strategy Leaves More Questions Than Answers

With the disclosure of Apple's new operating-system strategy (see page 5), the company has finally begun filling the strategic vacuum created when Copland was abandoned last year. Apple's plan deserves credit for being bold and innovative, but it also means Mac applications will never have the full benefit of a protected, multitasking operating system unless they are rewritten (though Apple is working on tools to ease this transition). The new OS, codenamed Rhapsody, is not an enhanced Macintosh but rather a new platform that offers Macintosh compatibility.

The success of the OS plan is also a critical issue for PowerPC: with Windows NT on PowerPC all but abandoned, the volume desktop future for PowerPC lies entirely with Apple's software. Unfortunately, the new OS strategy is unlikely to lead to significant market share growth for Apple. Furthermore, applications written for Rhapsody will be easily ported to other operating systems and processor architectures, reducing the proprietary lock PowerPC has had on Macintosh applications.

What does this mean for Mac users? For the next year and a half—or longer, if, as seems likely, the software schedule slips—Mac OS will continue to lack key modern OS features. Starting in mid-1998, Mac users will have the choice of staying with the old OS or moving to Rhapsody.

Rhapsody is sure to have far greater memory requirements than Mac OS; NextStep currently requires 32M, and it would not be surprising if Rhapsody requires significantly more to run well. This means the vast majority of the installed base of Macintosh systems will require memory upgrades to handle the new OS. Education and home users, long the core of Apple's market, may find the increased memory requirements to be onerous, if not prohibitive. Rhapsody will also require new drivers for peripherals, such as scanners and backup devices. Users with devices from companies that have disappeared, or that have dropped Mac support, may find they can't use these devices under the new operating system.

Most Mac OS applications will run within the so-called compatibility box, but all the limitations of the old OS remain. For example, any application can crash the entire compatibility box. The only improvement from the current situation is that just the compatibility box, rather than the entire system, would need to be restarted. Apple claims applications will run at least as fast in the compatibility box as under the native Mac OS, due to the faster underlying I/O structure and kernel.

To get the benefits of Rhapsody, applications must be written to the OpenStep APIs. OpenStep offers a very nice development environment, including a powerful set of Web development tools, but it is far outside the mainstream and has had little success outside of large corporate in-house developers. Apple hopes its evangelism and higher volumes will make OpenStep a far bigger success, but this remains to be seen. Apple is fragmenting its already modest market share into two APIs; developers targeting Rhapsody will have, at least initially, only a fraction of the already small Macintosh market share available to them.

The user scenario for switching to Rhapsody will be similar, in many ways, to the switch to Power Macs. At first, users will run most applications in the compatibility box and gain little benefit from the new platform. In time, more software (especially high-end applications, such as publishing and multimedia development tools) will become available in native Rhapsody versions. The big question is how long this transition will take—and indeed, whether the majority of applications will ever be ported to Rhapsody.

Apple has committed to supporting Next's existing products, which provide the OpenStep APIs on top of Windows NT and various flavors of Unix. If Apple continues to support OpenStep as a cross-platform API, it could increase developer appeal by enabling developers to support Windows NT and Rhapsody with the same effort. However, this would leave Rhapsody's applications undifferentiated. Apple could add features to Rhapsody without offering them in the NT version of OpenStep, which would provide differentiation for Apple but weaken the developer proposition.

Mac developers and users facing the tumultuous, multiyear transition to Rhapsody are likely to look more intensely than ever at shifting their efforts to Windows. Even if many applications move to the OpenStep APIs, users probably will have the option of running most of those applications under NT. Users of OpenStep applications will have a choice between an x86 system running NT, with the additional bonus of Windows applications, or a PowerPC system running Rhapsody, with the additional bonus of Mac applications.

Apple is, in essence, allowing Mac OS to slowly fade away while building its future on the Next platform. Although this strategy may enable Apple to build a sustainable niche, it pushes today's Macintosh even further into the fringe. M

Tillamook to Extend P55C

Sources have confirmed that Intel is developing a 0.25-micron version of its P55C processor, as we have speculated (see MPR 10/28/96, p. 20). The new device, said to be code-named Tillamook after a small town in Oregon, is expected to be a simple optical shrink of the current P55C processor. The P55C is built in Intel's 0.28-micron process, known as P854. We expect Tillamook to appear sometime in 2H97 at 200 MHz and possibly 233 MHz.

The key advantage of the shrink is a significant reduction in power. The 0.25-micron process, known as P856, is designed to run at 1.8 V (see MPR 9/16/96, p. 11), while the current P55C operates at 2.45 V in notebooks. This voltage change alone will decrease power dissipation by almost 50%. At 200 MHz, the P55C dissipates too much power to fit into a standard notebook design, preventing Intel from offering this part for mobile systems. Tillamook will easily fit into standard notebooks at 200 MHz.

In fact, even a 233-MHz Tillamook would have a maximum power dissipation of about 6 W, no sweat for notebook designers. Since the P55C hits 200 MHz in the current process, the smaller transistors should allow operation at 233 MHz. While a 233-MHz Tillamook would be a boon to notebook users, Intel may wish to push desktop users to the Klamath socket, locking out its x86 competitors. Intel may release the 233-MHz Tillamook only in a mobile module to keep it from appearing on the desktop.

Another advantage is a significantly decreased die size: Tillamook should be about 85 mm^2, just over half the size of the 140-mm^2 P55C. (Despite the 0.28-micron transistors, the P55C uses the equivalent of 0.35-micron metal layers, so the move to 0.25-micron produces a substantial die shrink.) This shrink will reduce manufacturing costs and increase per-wafer output.

Intel engineers will be challenged to provide 3.3-V I/O with the 1.8-V process, originally intended for 2.5-V I/O. Assuming Intel overcomes this challenge and that Tillamook maintains the P55C pinout, the only change required to the motherboard will be for the lower supply voltage.

Pressure from AMD and Cyrix may have helped Intel decide to greenlight the new chip. Tillamook gives Intel a response to the K6 and M2, which both offer increased performance in the P55C socket. The new part also provides some relief to thermally stressed notebook designers while filling a gap between the P55C and the forthcoming Mobile Deschutes, a P6 processor due in 1H98.

If Intel chooses to release a 233-MHz Tillamook for the desktop, it will provide one last performance kicker to the Pentium line before forcing vendors to move to P6 motherboards. As the first Intel processor to go through four full process generations, the Pentium core is proving to have quite a long lifetime. —*L.G.*

Intel Launches MMX, P55C

Capping a nine-month product roll-out, Intel has officially launched the Pentium Processor with MMX Technology, previously known as the P55C (see MPR 10/28/96 p. 20 and 12/30/96, p. 1). Intel has been shipping the chip in volume for some time, so both mobile and desktop systems using it are available immediately from a wide range of vendors.

The P55C delivers a modest performance benefit for applications that don't use MMX because of its larger on-chip cache. The 200-MHz chip delivers 6.4 SPECint95 (base) and 3.9 SPECfp95 (base)—an impressive boost of 26% over the non-MMX version (see page 27 for full SPEC details). On BAPCo's SYSmark32 tests, the 200-MHz P55C shows gains of 12% under Windows 95 and 19% under NT 4.0. These gains are lower than for SPEC because of the greater number of memory and I/O accesses in the application-oriented SYSmark32.

Intel's Media Benchmark—one of few benchmarks that illustrate MMX performance—shows a boost of about 60%. This is not a particularly meaningful number, however, as it is a combination of four widely varying results. On 3D geometry, which does not use MMX, the P55C delivers a trivial 4% increase, mainly due to the larger cache. On image processing, the improvement is a whopping 370%; audio shows a 113% gain, while video is boosted by 78%.

After January 27, pricing (in 1,000s) for the desktop version, which is in a plastic PGA and runs at 2.8 V, is $356 for the 166-MHz part and $539 for the 200-MHz version. The mobile versions are in PGA or TAB packages and operate at 2.45 V; pricing in either package is $539 at 150 MHz and $336 at 166 MHz.

The desktop prices are about $50 higher than those of the non-MMX versions at the same clock speed, while the 150-MHz mobile version carries a larger $122 premium. When one compares performance, on the other hand, the P55C-166 fares well against a Pentium-200 but costs $142 less. If buyers are savvy, this difference will cause the old 200-MHz part to phase out rather quickly.

The initial MMX software offerings are nearly all consumer focused. At the launch event, Intel showed about a dozen applications, including games, photo capture and editing programs, home 3D modeling software, and a software MIDI synthesizer. (See *mmx.com/mmx/software* for a list of applications.) Intel expects about 100 applications supporting MMX to ship by the end of the year.

The early applications are predominantly from smaller companies. To motivate these vendors to support MMX before there is any installed base, Intel has provided cash as prepaid royalties for system-bundling deals. In essence, Intel has guaranteed the software vendors a certain level of success in selling their applications to system makers for bundling, and it has provided the cash up front to help fund

development work. In return, the developers had to commit to implementing a certain level of MMX optimization.

Thanks to its lower supply voltage, the P55C is able to deliver more performance within a thermal envelope similar to the P54C's. The 166-MHz mobile version is rated at 9.5 W maximum, slightly less than the mobile P54C-150. . For the desktop versions, the power dissipation is also similar to that of the P54C: the 200-MHz P55C dissipates a maximum of 15.7 W. (See *developer.intel.com/design/mmx/index.htm* for more information.)

With most information on the P55C previously disclosed, the official launch provided few surprises. We expect the initial midrange pricing for the part to drop substantially by midyear, making the P55C the best-selling PC processor during 2H97. This growth will quickly establish MMX as a requirement in the PC market. —*M.S.*

Apple Offers New OS Strategy

Apple has, at long last, laid out its new operating-system strategy and taken the first step toward implementing that strategy by acquiring Next Software. Apple's plan leads to a modern, object-oriented operating system replete with all the right buzzwords. Unfortunately, the benefits of the new OS will accrue only to applications written for a new application programming interface (API) based on Next's OpenStep API. Macintosh applications will be supported only within a compatibility box that carries with it all of the disadvantages of the current Mac OS.

The new operating system, code-named Rhapsody, will include Next's OpenStep software, extended with a few key Mac APIs, such as QuickTime and OpenDoc, and a version of Mac OS for compatibility with existing applications. An early developer release is promised for the middle of this year, with a limited end-user release by the end of the year. A version with Mac application compatibility and an enhanced Mac-style user interface is promised for mid-1998. This version is expected to be the first of interest to Mac users; the late-'97 version will be used mainly by developers and current users of Next's software.

Next's original product was a full operating system, called NextStep, based on the Mach kernel (used in a version of Unix developed at Carnegie-Mellon). More recently, Next shifted its efforts to OpenStep, a "middleware" product that implements Next's development environment and APIs on top of existing operating systems (including Windows NT and various versions of Unix). Although it has been assumed in many press reports that Rhapsody will use the Mach kernel, Apple says this decision has not been made; the Copland kernel and other options are also being considered.

With the now-abandoned Copland operating system, Apple had hoped to provide a high degree of compatibility with existing Mac applications while replacing the kernel to provide memory protection and pre-emptive multitasking. Because Mac Toolbox routines are not re-entrant, Copland required a nearly complete rewrite of the operating system. Unfortunately, most Mac applications use undocumented features in the system software, such as directly accessing internal data structures. This misuse has made maintaining compatibility extremely difficult.

The new strategy forces existing Mac OS applications to run within a "compatibility box," which is just a copy of Mac OS running as a task under the new operating system. This version of Mac OS will be modified to work through the new kernel instead of communicating directly with the hardware. Apple says application compatibility will be better than it would have been with Copland, and at least 85% of existing applications should run. A key difference from the Copland strategy, however, is that standard Macintosh applications cannot take advantage of the new pre-emptive multitasking and interapplication memory protection.

Apple promises that twice-yearly releases of the existing Mac OS will continue through at least the end of the decade. The Harmony release (Mac OS 7.6), just now shipping, has modest stability and performance enhancements. Due in mid-'97 is the Tempo release, which will include a new multithreaded Finder—finally written in native PowerPC code—that will bring to System 7 some of the user-interface enhancements originally created for the ill-fated Copland. For most Mac users, Tempo and its follow-ons—rather than Rhapsody—will be the most significant developments for at least the next two years. —*M.S.*

AMD Pushes K5 to PR166 Performance

By increasing the K5's core clock speed to 116.5 MHz (see MPR 12/9/96, p. 4), AMD has announced a new version with performance similar to that of a Pentium-166, according to AMD. The new K5-PR166 is slated for availability by the end of this quarter. AMD is currently shipping K5 processors with performance ratings of up to PR133, using internal clock speeds of up to 100 MHz. The PR166 carries a list price (in 1,000-unit quantities) of $167.

Reaching the PR166 level puts AMD well into the sweet spot of the PC market. Pentium-166 systems were the most popular high-end PC during the recent Christmas season; with the introduction of the P55C, the Pentium-166 will be Intel's midrange processor throughout 1H97. The PR166 lists for 43% less than the Pentium-166, and AMD is likely to offer deeper discounts than Intel.

On the other hand, a large gap in Intel's pricing structure puts the PR166 at about the same price as a 150-MHz Pentium and $33 more than a Pentium-133. OEMs will gain little extra performance by substituting a PR166 for an Intel processor of the same price.

For the first time, AMD has introduced a version of the K5 that matches the performance of an Intel chip priced at more than $200. This success will boost AMD's average selling price and aid in the company's recovery from a financially disastrous 1996. The K5, however, is still far from matching the performance of Intel's fastest parts, a task that falls to the forthcoming K6. —*L.G.* M

RISC Processors

Continued from page 1

Any such speed boost will have to last until the end of the year, when the 21264 is set to debut. Digital claims the forthcoming device will achieve a stunning 30 SPECint95 and 60 SPECfp95 (base), making it the **World's Fastest Microprocessor (announced)**. These figures represent more than twice the performance of the fastest chips today and, if achieved, should keep Digital in the performance lead.

To date, however, this lead has not led to a large market share for Alpha. Digital's hopes for a significant increase in volume lie with Windows NT. The vast majority of NT users continue to work with x86 systems, as most NT customers are buying systems for $4,000 or less. Few Alpha systems are available at this price today, but Digital plans to change that with the 21164PC, a stripped-down version of the 21164 that supposedly retains that chip's superior performance while using PC-style cache and memory chips. Digital may need a **Bit of Magic Dust** to deliver on this claim; if it does, users willing to consider a non-x86 processor will find the 21164PC a solid competitor for Klamath in the high-end NT market.

Contrary to our projections, Mitsubishi stayed aboard the Alpha ship despite another year of essentially no Alpha revenue. The company is a codeveloper and second source of the 21164PC and thus could take advantage of any NT gains. The potential for NT-on-Alpha also attracted newcomer Samsung to the fold. The Korean giant will initially focus on the 21264 core but may try to muscle in on the 21164PC action. By 1998, Mitsubishi could get **Caught in a Squeeze Play** between Samsung's low manufacturing costs and Digital's developed sales channels.

The second prong to Digital's NT strategy is FX!32. This emulation/translation software wins our **Alchemy Award** as the best product yet to convert x86 code into RISC. Although much delayed, FX!32 finally achieved open availability last fall. At least by some measurements, the product achieved its goal of delivering 70% of native Alpha performance when running translated x86 programs. FX!32, combined with native versions of Microsoft Word and Excel as well as many performance-hungry applications, will help wean some NT users from their x86 systems.

For Alpha to succeed, particularly from the viewpoint of Mitsubishi and Samsung, the platform must ultimately attract more system vendors. The Silicon Graphics purchase of Cray, which will ultimately replace the Alpha chips in Cray's MPP system with MIPS processors, leaves Digital as the only Alpha system vendor most people have ever heard of. To make its chips more attractive, Digital has given up its title as maker of the **Most Expensive Microprocessors**. As we recommended last year, the company cut its processor prices in half, bringing them more in line with Intel's.

Any meaningful financial benefits from the NT strategy are unlikely to accrue before 1998. The Alpha vendor must find some other way to stem its recent flow of red ink before the wave drowns corporate interest in Digital products.

PowerPC Resets Goals

During the past year, IBM Microelectronics and Motorola got their act together, taking advantage of new manufacturing processes to aggressively increase the clock speeds of their mainstream PowerPC chips. With both companies shifting most of their production to 0.35-micron CMOS, the 603e climbed to 240 MHz while the 604e reached 225 MHz, earning the rarely seen **Ahead of Schedule** award. The vendors also reined in their marketing groups, not announcing products until they were actually shipping, for a change.

Unfortunately, this success did not extend to the ill-fated PowerPC 620. This chip, originally due in 3Q95, wins the **Flying Dutchman** award: doomed to roam the seas forever, occasionally glimpsed through the mist but never finding its way to port. The latest plan has the 620 showing up in IBM systems sometime in 2H97—maybe. Users needing 64-bit support may instead turn to IBM's Apache, an internally developed 64-bit PowerPC processor. This would leave Groupe Bull as the only customer for the 620.

After reaching the end of the original PowerPC roadmap (except for the aforementioned Dutchman), Motorola and IBM unfurled a new map that extends through 2001, giving them the **Biggest Crystal Balls** award. This year will see the debut of the first G3 processors, which are derived from the 603 and 604 cores but add new cache and bus interfaces to increase performance. The G4 is due in late 1998, and the 2K is planned for 2001.

Despite recent advances, PowerPC has little hope of establishing a significant performance advantage over Intel's processors. And while every other major processor vendor is adding multimedia extensions, the PowerPC partners refuse to even acknowledge a plan to implement them, earning the partners a dubious **Mental Eclipse** award. This blind spot will put PowerPC chips well behind Intel's MMX processors in performance on many multimedia applications.

IBM rolled out its P2SC, a single-chip version of its Power2 processor, last fall. The massive chip wins several awards, including **Most Transistors** (15 million), **Best Memory Bandwidth** (2.2 Gbytes/s), and on the downside, **Highest CPU Manufacturing Cost** ($375 estimated). The six-way superscalar POWER processor offers pedestrian integer performance but superlative speed on high-end scientific code and high-bandwidth commercial applications such as OLTP.

Newcomer Exponential unveiled its x704, due to ship in 2Q97. The PowerPC chip uses bipolar logic to achieve clock speeds of up to 533 MHz and better projected performance than any PowerPC processor from Motorola or IBM. We give this chip the **Light Bulb** award, in honor of its good ideas and its power dissipation (85 W). Apple and others will use this chip in high-end Macintoshes.

Even as the PowerPC hardware plot improved, the software story descended into lurid prose. PowerPC wins the

award for **Most Dead Operating Systems**, as IBM dropped OS/2 support, Sun de-emphasized Solaris for PowerPC, and Windows NT on PowerPC is left with no announced system vendors. The once all-consuming PowerPC universe has essentially collapsed to proprietary IBM operating systems (AIX, OS/400) and Mac OS.

Despite the dire straits of its own company's processor, IBM's PC group continues to thwart every attempt to leverage its sales channels in support of PowerPC, earning the **Barry Bonds Poor Teammate** award. IBM has a license to sell Mac clones and could become the first major PC maker outside of Apple to adopt Mac OS, but don't expect to see this happen any time soon.

With the evaporation of NT support, major vendors such as Canon and Toshiba have abandoned the PowerPC ship. Although Apple finally opened its Mac OS licensing campaign early last year, it was a case of **Right Place, Wrong Time**. The unimpressive results are that Macintosh clones are available from Motorola and a handful of small companies that few non-Mactivists would know.

The inability of IBM and Motorola to deliver significantly better performance or price/performance than Intel has led to this lack of interest. Recent improvements are simply **Too Little, Too Late**. There remains little reason to use PowerPC for any software that already runs on x86. At this point, PowerPC's market share is tied to Mac OS, the one operating system that doesn't run on x86. Apple's ongoing problems, however, have caused the Mac's market share to drop from about 10% to 7% in the past year, as forecast by Nick Tredennick (see MPR 9/12/94, p. 18).

We're not sure what to make of Apple's new OS strategy (see page 5). If the plan fails, Apple's share will continue to plummet, although the Mac faithful may keep the company alive indefinitely. But even in the best case, a revived Mac OS, along with the next-generation Rhapsody OS, seems unlikely to exceed a single-digit market share. Interestingly, Next's OS has already been ported to x86; we would not be surprised to see Rhapsody on x86 or IA-64 as well as on PowerPC.

Many pundits, including ourselves, had forecast that PowerPC could achieve a 20% share of the desktop market by 2000. Now, it looks like PowerPC will be lucky to own 5–10% at that point. This share is still far better than that of any other RISC and is plenty to keep the architecture afloat, but it won't threaten Intel and, compared with the initial bright hopes for PowerPC, is a **Major Disappointment.**

HP Regains Performance Competitiveness

As Figure 1 shows, HP started 1996 trailing the other major processor vendors, including Intel, in integer performance. The debut of the PA-8000 in April changed all that, pushing HP into the lead in both integer and floating-point performance and completing a **Worst-to-First Leap.** Although the 500-MHz 21164 later surpassed HP's integer score and matched its floating-point score, the PA-8000 remains ahead of all other shipping microprocessors.

Major RISC Events of 1996

Digital's 21164 rocketed from 333 MHz (2/12/96, p. 4) to 400 MHz (3/5/96, p. 4) and then 500 MHz (7/8/96, p. 1). The company also revealed its superfast 21264 (10/28/96, p. 11). Samsung signed on as a third source for Alpha processors (7/8/96, p. 4). Digital cut its processor prices in half (12/30/96, p. 5).

Digital gave a peek at its low-cost 21164PC (4/15/96, p. 4 and 10/28/96, p. 4). The chip will be the first with Alpha's multimedia extensions (11/18/96, p. 24). The company's FX!32 emulator/translator (3/5/96, p. 11) began shipping in the fall (10/28/96, p. 4).

Exponential taped out its BiCMOS PowerPC chip in January (2/12/96, p. 6) and described its internal architecture at the Microprocessor Forum (10/28/96, p. 1).

The **PowerPC** 604e jumped to 180 MHz (5/6/96, p. 4), then eased up to 200 MHz (5/27/96, p. 13) and ultimately 225 MHz (8/5/96, p. 5). The PowerPC 603e used a shrink to 0.35-micron CMOS to reach 200 MHz (5/27/96, p. 13) and later 240 MHz (10/28/96, p. 5).

Motorola and IBM jointly revealed a new PowerPC roadmap (8/26/96, p. 12).

Apple expanded its Mac OS licensing program by allowing Motorola (3/5/96, p. 4) and IBM (5/6/96, p. 11) to sublicense the OS to third parties. By year end, seven companies had licensed Mac OS (10/7/96, p. 5).

IBM began shipping its P2SC processor in August (8/26/96, p. 14) and outlined plans to deploy a 64-bit Apache processor in mid-1997 (3/25/96, p. 4).

HP shipped limited volumes of the PA-8000 in April (4/15/96, p. 4), seizing the performance lead from Digital. PA-8000 workstations followed in June (6/17/96, p. 4). HP revealed plans for the PA-8200 and 8500 at the Microprocessor Forum (10/28/96, p. 18).

MIPS announced MIPS V and MDMX (11/18/96, p. 24). R10000 servers began shipping in March (2/12/96, p. 4), but workstations didn't ship until the fall (10/7/96, p. 5). The R5000 was announced at 200 MHz (1/22/96, p. 10) but shipped at 180 MHz (2/12/96, p. 4).

QED announced plans to sell its own chips (9/16/96, p. 5) starting with the RM7000 (10/28/96, p. 36).

Fujitsu's TurboSparc (11/18/96, p. 17) began shipping as a successor to MicroSparc-2. **Sun** revealed plans for UltraSparc-2i (10/7/96, p. 1), which will fill in the low end starting in late 1997.

Netpower dumped MIPS in favor of **Pentium Pro** (3/5/96, p. 5). Amdahl chose Pentium Pro over RISC (5/27/96, p. 4). Compaq rolled out its first workstations, all based on Pentium Pro (9/16/96, p. 5).

Microsoft dropped support for **Windows NT** on MIPS (10/28/96, p. 5). IBM and Motorola extinguished NT on PowerPC (12/30/96, p. 4).

The PA-8000 is an impressive device. With a buffer of 56 instructions, it has the **Most Reordering Capacity** of any microprocessor (see page 27). Its dual floating-point multiply-accumulate units are also unique. All this power comes at a price: at 345 mm^2 in an antiquated 0.5-micron process, the PA-8000 also takes the award for **Biggest Die.**

The company plans to stay in the performance race with a pair of processors derived from the PA-8000. The PA-8200, due this spring, will boost performance by about 40% with a few relatively small changes and a clock-speed boost. As Figure 2 shows, this chip should give HP leadership FP performance, at least until the 21264 appears. The PA-8500, planned for mid-1998, will challenge the 21264's performance using a 0.25-micron process. The 8500 will fill the gap until Merced appears in 1H99.

HP started shipping its new midrange processor, the PA-7300LC, in September. The chip delivers performance similar to that of a 200-MHz Pentium Pro (a bit better on FP, a bit worse on integer). HP itself is now selling Pentium Pro workstations, preparing for the ultimate unification of its product lines around Merced and other IA-64 chips. While the company has a solid plan to address the high end, efforts on IA-64 may prevent progress in the midrange; the 7300LC is probably the last PA-RISC chip to address that space. Well before Merced appears, many HP customers will be faced with the choice of paying a premium to stay with PA-RISC or getting maximum price/performance by adopting Pentium Pro. At least HP can make a sale in either case.

Silicon Graphics Revamps Products

SGI spent the year reworking its entire system lineup, moving to the R10000 at the high end and the R5000 at the low end. Both chips provided performance disappointments, earning MIPS a penalty for **Elastic Marketing Claims.** The R5000 was announced at 200 MHz but never got past 180 MHz in SGI's systems. Performance fared worse, as the announced 5.2 SPECint95 (base) turned into 4.0 when systems rolled out, although it later crept up to 4.7. The chip is now shipping at 200 MHz in embedded applications but not in workstations.

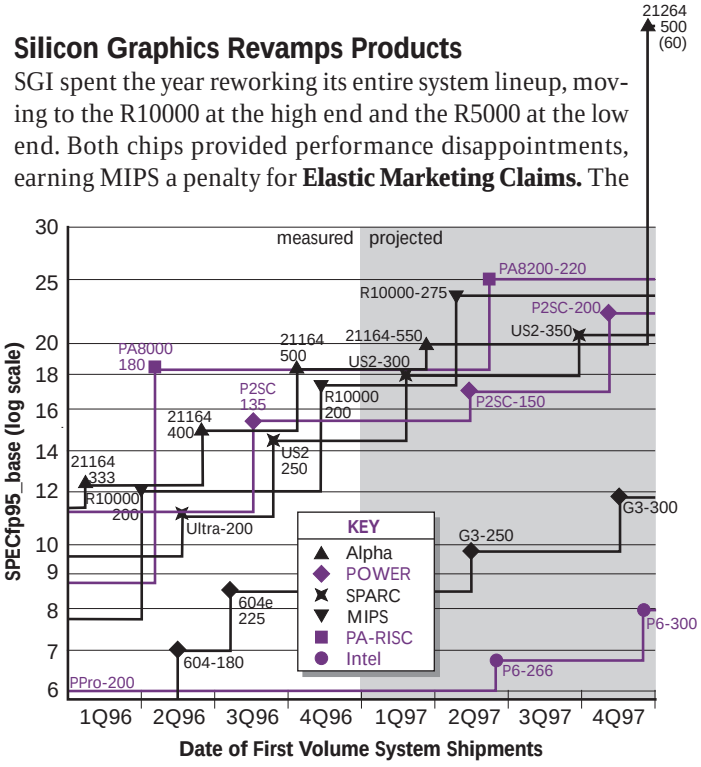


Figure 2. HP is tied for the FP performance lead with Digital and hopes its PA-8200 will reign supreme during 2H97. (Source: SPEC for 1996 data, MDR for 1997)

The R5000 offers significantly lower performance than a Pentium Pro, even on floating-point code, but it costs much less to manufacture. In fact, at just $25, the R5000 has the **Lowest Manufacturing Cost** among all desktop RISC processors. Although this low cost will ultimately aid the R5000 in the embedded market, it does little to help SGI.

The R10000 rolled out in 1Q96, but yield problems prevented the processor from achieving significant volume until the fall. NEC and Toshiba continue to be unable to get more than a few parts to yield at the advertised 200 MHz, although there are enough 195-MHz parts to enable SGI to ship some high-end servers at that speed. These yield problems caused the price of the 200-MHz R10000 to remain at $3,000, making it the **Most Expensive Microprocessor.**

The R10000 had its own performance disappointment: the initial systems were rated at 13 SPECfp95 (base), far short of the 18 originally promised. MIPS explained that system limitations were hampering performance, and by the end of the year, new systems appeared that demonstrated the "true" performance of the R10000 is 17.4 SPECfp95. A final blow was NEC's manufacturing problem that forced it to recall the few thousand R10000s it had shipped, earning the **Most Embarrassing Bug** award.

The past year also saw the demise of Windows NT on MIPS, a promising product cruelly ignored by MIPS parent Silicon Graphics. Earning a **Squandered Advantage** penalty, SGI's complete disdain for NT drove Acer, NEC, and ultimately all other NT-on-MIPS system vendors from the market, leaving Microsoft no choice but to pull the plug, despite having originally developed NT on MIPS systems.

In 1997, SGI will look to the RM7000 to revitalize its midrange. This chip, the first sold under the QED name, is projected to deliver in excess of 10 SPECint95 and 10 SPECfp95, keeping pace with Intel's high end. The R10000 should see a shrink to 0.25-micron in 1H97, boosting the clock speed to 275 MHz and keeping SGI in the performance race with other high-end RISC vendors.

Sun Focuses on Java

It seems an odd match, but we are giving Sun the **Silent Running** award for saying so little about SPARC during 1996, at least in part because the Java spigot was on full (see page 16). One minor misstep: Sun Microelectronics (SME) announced a 182-MHz version of UltraSparc that never shipped; the vendor jumped directly to 200 MHz a quarter later.

In a bigger snafu, SME claimed UltraSparc-2 was shipping in volume at 250 MHz back in June, yet to date the part has appeared in only a few expensive Sun servers for which no benchmarks have been published, earning UltraSparc-2

a **Phantom Product** citation. The culprit appears to be Texas Instruments' manufacturing process, as the UltraSparc-2 design has been complete for months. TI's aggressive plans to advance its IC process technology (see MPR 9/16/96, p. 11) seem to be falling short.

Even if we give Sun credit for the estimated performance of its 250-MHz part, the company languishes in its traditional role of sporting the **Slowest High-End Processor**. If TI can get back on track, UltraSparc-2 may reach 350 MHz this year, but this improvement will be merely enough to compete with Intel's Klamath and the PowerPC G3 for last place in the integer performance race.

Throughout 1996, Sun Microsystems (SMCC) relied on the skanky MicroSparc-2 (1.4 SPECint95) to "power" its low-end and midrange workstations. SMCC recently rolled out systems based on Fujitsu's new TurboSparc chip, which offers twice the performance of MicroSparc-2 but still lags well behind Pentium, much less Pentium Pro, in performance. To gain a competitive low end, Sun needs to move to UltraSparc-2i, a highly integrated derivative of UltraSparc, but this chip isn't due until late 1997 or early 1998.

SMCC's adoption of UltraSparc ended its brief flirtation with Ross Technology's HyperSparc CPU. This loss, coupled with the erosion of the SPARC clone market, left Ross reeling; expenses exceeded revenues by more than 30% in the most recent quarter. Apparently, Ross didn't expect Sun to cut off its purchases of HyperSparc, earning the Texas vendor the **Jeane Dixon Forecasting** award.

Intel Gains Despite Slips

In a change of style, Intel rolled out four speed grades of its new Pentium Pro processor in late 1995 rather than doling them out one per quarter. This strategy vaulted Intel into the integer performance lead, albeit briefly, and garnered plenty of attention. For 1996, however, we are flagging Intel for **Illegal (Lack of) Motion,** as the 200-MHz Pentium Pro remained its high-end processor for the entire year. This inactivity leaves Intel well behind Digital and HP—and, to a lesser extent, MIPS and PowerPC—in integer performance, although Intel still leads the laggard SPARC.

Things are looking better for 1997. The next P6 processor, Klamath, is expected to appear in 2Q, boosting clock speeds to 266 MHz. Faster clock speeds await the deployment of Intel's 0.25-micron process, due in 2H97. We expect to see the P6 hit 300 MHz by the end of this year, but even this improvement will not allow Intel to approach the performance lead in 1997.

Intel's only new desktop processor for most of 1996 was the 200-MHz Pentium. Introduced with "immediate availability" in June, the chip was extremely difficult to find in systems until well into the fall, earning Intel a **Phantom Product** citation. Intel denies any production problems; the good news is that the chip is now widely available.

Despite these problems, even the 1995-vintage Pentium Pro was enough to disrupt RISC vendors' plans. Earning an **Operation Crush** award, the chip delivered enough performance to block MIPS and PowerPC from gaining NT design wins, as vendors from Amdahl to Netpower chose Pentium Pro over RISC chips. Only Alpha, with its superior performance, remains to challenge Intel in the NT space.

These NT vendors represented only incremental business to RISC chip vendors, so losing them does little harm. Pentium Pro's real threat is against the RISC workstation and server businesses that form the heart of the revenue streams of Sun and Silicon Graphics. This threat is exemplified by Compaq's entry into the workstation market, with its lineup based entirely on Pentium Pro and Windows NT. These systems offer performance (integer, floating-point, and 3D graphics) similar to that of low-end and midrange RISC workstations but, taking advantage of PC components and economies of scale, at significantly lower prices.

Leveraging their own PC businesses, Digital and HP are now offering similar Pentium Pro workstations, using the **Eat Your Own Young** strategy popularized by Intel. Sun and SGI, however, have no such alternative; their low-end and midrange business appears doomed. Sun is trying to reinvent itself as a high-end-server and thin-client vendor, while SGI appears to be positioning itself as a high-end 3D and supercomputer company. Both companies see Web servers as a major market opportunity, although Pentium Pro will provide competition there as well. We believe these tricky business conversions will limit growth for at least the next few years, making it more difficult to support in-house RISC architectures such as SPARC and MIPS.

Intel Challenges Cozy RISC Vendors

Within the cozy confines of the RISC enclave, 1997 appears devoid of earthshaking events. Digital and HP will vie for the performance leadership crown. Quarter-micron versions of the R10000 and UltraSparc-2 will improve the competitiveness of these parts. PowerPC and Intel will trail in performance, particularly on floating-point applications, but the gap on integer code will not be as great as in the past. No new processor cores are slated to appear from the major vendors until the debut of the 21264, likely to be at the very end of the year (or later). When it appears, the forthcoming Alpha chip will open an enormous performance gap.

Among customers considering either RISC- or Intel-based systems, however, the plot is more likely to resemble that of *Mars Attacks!*, with the P6 playing the role of the little green men. The combination of the P6 and Windows NT delivers a price/performance advantage over RISC/Unix systems, and the P6, particularly in low-cost dual-processor configurations, can match the performance of all but the fastest RISC systems on most tasks. Because of the high degree of software lock-in among RISC users, this effect will not vaporize any RISC vendors overnight, but it will place a drag on sales and particularly on profits. As in *Independence Day*, RISC vendors must devise an innovative solution to thwart an incredibly powerful and aggressive foe. M

First Media Processors Reach the Market

Programmable Solutions from Chromatic, Philips Gain Momentum

by Peter N. Glaskowsky

Despite limited availability in 1996, media processors became a significant factor in the PC market. Several new architectures were introduced in 1996. There are now three major architectures for the PC market, and designers of consumer electronics have several to choose from.

Most of the activity was behind the scenes: building strategic relationships between hardware and software vendors and attempting to influence the development of 3D and multimedia architectures at Microsoft. These efforts will guide the formation of the market over the next few years.

This year will be much busier than last, as the plans of several vendors finally reach fruition and customers get their first look at the new technology. Products based on Chromatic's Mpact will hit the streets this month or next, with the Philips TriMedia only three months behind. Samsung's more ambitious MSP should arrive late in the year, finally allowing direct comparisons among the three chips based on real applications instead of raw clock rates.

While these three vendors are hoping to gain design wins in both PCs and consumer products, other vendors are more narrowly focused on consumer devices. By eliminating some of the overhead required by PCs, such as floating-point support and a PCI interface, these embedded chips aim to reach the lower price points required for consumer products. Fujitsu and Mitsubishi have announced such devices, with DVD players as the primary target; Oak and C-Cube are expected to follow suit this year.

Rendition is in a class by itself. With its programmable core, the Vérité chip looks much like other media processors, but the company has positioned the device solely as a 3D accelerator for PCs. Vérité competes mainly against hardwired 3D graphics chips.

Combining Capabilities Can Cause Confusion

Flexibility, the greatest advantage of media processors, may also be their biggest problem. In some ways, media processors are a middle-of-the-road technology. In theory, they combine the cost/performance advantages of hardwired solutions with the flexibility of software implementations. This opens them to competition from several directions, however. Makers of hardwired graphics and audio chips, along with software-only vendors, can target specific aspects of PC multimedia and sometimes offer better point solutions.

The media-processor solution does not satisfy all PC OEMs. Some system vendors believe that the classic approach, with separate subsystems for graphics and audio, provides a more useful form of flexibility. By offering a selection of graphics solutions—a low-end 2D/3D chip on the motherboard, or a few different PCI cards—as well as hardware and software alternatives for audio, vendors can create a well-differentiated product line. Media-processor boards can be difficult to fit into this strategy. Even though media processors can provide high-performance graphics along with high-quality audio, they potentially eliminate several configurations from a system vendor's product line.

This problem is really the result of the checklist mentality that prevails at many PC vendors. Product differentiation is achieved by checking off a different set of items—3D acceleration, MPEG playback, wavetable audio, etc. Media processors are just too good at this game: they allow the vendor to check off every box, as long as the media processor has the right software available.

The narrow checklist view makes media processors look so good that vendors have a hard time explaining why the user should want any other system configuration. The solution to this quandary is to offer media-processor solutions at several performance levels. Low-end and midrange systems can be differentiated solely by the software components sold with the system, while high-end systems can be equipped with faster hardware and even more software.

Chromatic to Take Early Lead

The first full-featured media processor to ship will come from Chromatic Research. Chromatic's two original partners, Toshiba and LG Semicon, shipped the first production units of the Mpact/3000 media processor to OEMs in September of last year. In November, SGS-Thomson became the third (and final, according to Chromatic) source for Mpact. SGS-Thomson is likely to begin shipping product in late 1997.

The key strengths of first-generation Mpact parts are in the areas of 2D graphics, audio, and MPEG-2 playback. Mpact's 3D performance will improve dramatically with the arrival of floating-point hardware and a rendering pipeline on Mpact 2, but Mpact/3000 is at least competitive with low-end 3D chips like the S3 Virge and ATI Rage.

No Mpact-based products have yet appeared in retail sales channels, and only LG Electronics has even announced a board-level Mpact product. Even so, Chromatic anticipates strong sales this year, primarily in motherboard applications. The Mpact R/3000 and R/3600 are expected to ship in volume in 1Q97, adding an internal RAMDAC and a faster speed grade, with the Mpact 2/6000 shipping in 3Q97. This lineup will give Chromatic customers four parts to choose from, providing much-needed product-line differentiation.

	Chromatic Mpact R/3000	Chromatic Mpact 2/6000	Philips TM-1	Philips TM-PC	Samsung MSP-1	Samsung MSP-1G
2D acceleration	Yes	Yes	No	Yes	No	Yes
3D geometry (polys/s)	n/a	1M	750K	750K	750K	750K
3D setup (polys/s)	n/a	1.2M	1M	1M	750K	750K
3D fill rate (pixels/s)	5M	42M	n/a	n/a	n/a	n/a
MPEG-1 decode	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)
MPEG-2 decode	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)
MPEG-1 encode	Yes (HW)	Yes (HW)	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)
Videoconferencing	Yes	Yes	Yes (SW)	Yes (SW)	Yes (SW)	Yes (SW)
Video in	Yes	Yes	Yes	Yes	Yes	Yes
Video out	Yes	Yes	Yes	Yes	Yes	Yes
Audio support	Yes	Yes	Yes	Yes	Yes	Yes
Telephony support	Yes	Yes	Yes	Yes	Yes	Yes
Clock rate	62.5 MHz	125 MHz (est.)	100 MHz	100 MHz	100 MHz	160 MHz
Integer ops/cycle	48	48	38	38	64	64
Peak integer perf	3.0 GOPS	6.0 GOPS	3.8 GOPS	3.8 GOPS	6.4 GOPS	10.2 GOPS
Int width at peak perf	8 or 9 bits	8 or 9 bits	8 bits	8 bits	8 bits	8 bits
Peak FP performance	n/a	0.5 GFLOPS	0.5 GFLOPS	0.5 GFLOPS	1.6 GFLOPS	2.5 GFLOPS
Local RAM bandwidth	500 Mbyte/s	1200 Mbyte/s	400 Mbyte/s	400 Mbyte/s	800 Mbyte/s	1280 Mbyte/s
Open SW dev env	No	No	Yes	Yes	Yes	Yes
Price for chip	$50	n/d	$50	$53	n/d	n/d
Production date	Now	n/d	Now	8/97	3Q97	n/d

Table 1. Samsung's MSP-1 shows a clear advantage in both integer and floating-point performance compared to other PC media-processor architectures, while Chromatic's Mpact includes the broadest range of features. n/a=not applicable, n/d=not disclosed (Source: vendors)

Introducing second-generation Mpact technology even before first-generation parts had reached the hands of end users was a gutsy but correct decision. Chromatic is a small company, and Mpact 2 should reassure potential customers that Chromatic is determined to become a significant force in the PC market.

Software, Business Models Evolve

High-performance media processors mean nothing to end users without software to implement the necessary multimedia algorithms. Chromatic refers to this code generically as Mediaware, and derives most of its revenue from Mediaware licensing. Licensing fees for chip designs are calculated to cover the cost of chip development, not to generate profit.

Chromatic has released version 1.0 of its Mediaware library, which supports basic 2D, 3D, audio, telephony, and digital-video functions. The company has already described some of its plans for the next release in 1H97, adding DVD support, videophone operation, and more advanced audio and telephony features. This next release will also take advantage of MMX extensions, if present, to reduce host-processor overhead. All of this work is being done by Chromatic's 100+ software engineers, certainly a challenging task.

Chromatic does not make it possible for its semiconductor partners, or anyone else, to develop software for Mpact, although the company remains open to the possibility if a compelling case is offered for some specialty function. Aside from business issues, developing for a complex VLIW (very long instruction word) SIMD (single-instruction multiple-data) architecture is inherently difficult. If Chromatic were to allow third-party software development, it would have to expend considerable effort on tools, training, and technical support for the independent developer.

TriMedia Provides First Competitor to Mpact

The Philips TriMedia TM-1 is close on the heels of Mpact. Entering production only three months later than the Chromatic design, the TM-1 offers potentially better performance at a higher cost. As Table 1 shows, the chip's processor core is more directly comparable to the Mpact 2's, since it includes floating-point support. Both use VLIW and SIMD techniques to achieve high performance on multimedia algorithms.

Philips, however, chose not to include hardware support for 2D/3D graphics or MPEG encoding in the TM-1. While the TM-1 is nominally capable of acting as an SVGA-compatible display controller with the appropriate firmware, performance is likely to be unacceptably slow in this mode, and Philips does not emphasize this capability. Later TriMedia parts will remedy this omission.

In fact, Philips's roadmap refers to no fewer than seven TriMedia derivatives, as Figure 1 shows. By the end of 1997, Philips may be shipping the TM-1 (itself a shrink of previous internal versions), a TM-1c with further feature shrinks, a TM-PC for Microsoft's Talisman, and a TM-CE version for consumer-electronics applications. In 1998, Philips expects to have a TM-2 with 4× the performance of the TM-1 and additional (but unspecified) features. TM-2 will beget TM-TV, a version for interactive televisions from the Philips consumer-electronics division. An even faster part, described only as TM-3, may arrive in 1999.

In other respects, the TM-1's level of integration is similar to that of Mpact 2, with digital audio and video I/O. The

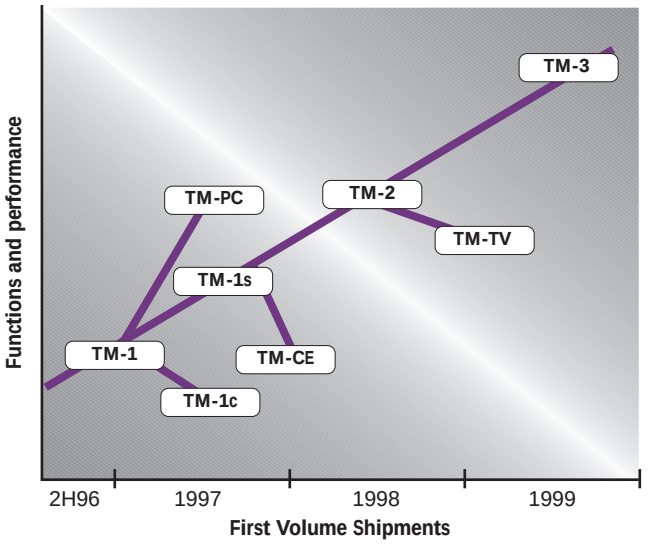


Figure 1. Philips's Trimedia roadmap shows a plethora of parts, including the mainline of TM-1, TM-2, and TM-3 as well as several derivatives aimed at specific markets. (Source: Philips)

Philips TM-1 reference design emphasizes these features, providing video digitizing and playback plus sound and telephony features. Most TM-1 products will follow the same pattern, leaving 2D/3D graphics on the motherboard or a separate expansion card.

Apple's recent adoption of TriMedia fits well with the part's current capabilities. This plan is similar to Apple's earlier use of a DSP for QuickTime acceleration. The coprocessor approach was dropped when Apple moved from the 68K to PowerPC, but now it's back. TriMedia thus becomes Apple's response to Intel's MMX. IBM, Motorola, and Apple have not developed multimedia extensions for the PowerPC processor family, so Apple was forced to find another way to provide multimedia acceleration for its platform.

Samsung Promises Best Performance

The most ambitious media-processor design yet described is Samsung's MSP. Although the first 100-MHz MSP is not scheduled to ship until 3Q97, Samsung has already described a 166-MHz follow-on that will exceed 10 BOPS on 8-bit data. Even the 100-MHz part matches the integer performance of Mpact 2 in the same time frame.

MSP shines in floating-point throughput. Its 256-bit-wide SIMD engine—four times wider than Mpact's—supports a 32-bit IEEE-compliant floating-point representation in addition to the 8-, 16-, and 32-bit integer formats common to most media processors. The result is a peak execution rate of 1.6 GFLOPS on multiply-accumulate operations at 100 MHz, far exceeding the FP capabilities of all other announced parts, as Table 1 shows. Floating-point performance translates directly to 3D geometry performance, giving MSP a significant advantage over host-based geometry processing and other media processors on complex 3D scenes with many small triangles.

Samsung sidestepped another problem faced by other media-processor vendors: the inefficiency of scalar tasks like communications and scheduling on vector processors. Instead, MSP includes an independent ARM7 processor core to handle system-level tasks like scheduling and host communication without interfering with the vector processor.

Talisman Offers Opportunity for TriMedia, MSP

Although Philips and Samsung plan to add limited 2D and 3D support to future versions of their media processors, the best opportunity for market-leading 3D performance for both architectures will come from Microsoft's Talisman initiative. Talisman defines a radically new 3D rendering architecture with chunk-based rendering and dynamic image-layer compositing. Aimed at the entertainment-software market, Talisman's enhancements should yield dramatically higher 3D throughput.

Microsoft's Talisman reference design will use TM-PC to accelerate 3D geometry calculations as well as audio and video operations, creating a comprehensive single-board multimedia solution that places very little demand on the host CPU except for scene definition and data-structure maintenance.

Samsung's MSP is also part of the Talisman program, but MSP's schedule is far enough behind the TM-1's that Microsoft has settled on TM-1 for the first reference design. Samsung will produce its own reference design once MSP is ready, giving software vendors two Talisman platforms to choose between.

Talisman is unlikely to have much effect on the market in 1997; we estimate fewer than 100,000 Talisman cards will be sold this year at an average price of at least $600, mostly to software developers and forward-looking end users. Throughout the year and into 1998, however, Talisman will be a powerful influence on the development of 3D software as well as competing 3D hardware. Chromatic, for example, has emphasized that Mpact 2 will support some Talisman features.

TriMedia, MSP Rely on Third-Party Developers

Philips and Samsung are also doing most of their own software development, but both depend on outside vendors for key software components. Philips provides TriMedia's real-time kernel and what Philips describes as a "smart" C/C++ compiler that understands the complex static scheduling rules in TM-1. This compiler, part of a software-development environment that Philips offers for $15,000, has been under development for seven years, and Philips believes it represents a significant edge over its competitors. The compiler comes with code libraries for many common multimedia algorithms, but Philips expects its OEM partners to differentiate their offerings by developing custom software.

Most of Samsung's software tools were developed under contract by Metaware. That company, mostly known as a tools developer for embedded development, provided a

Microsoft's Direct3D Delayed—ISVs Eye OpenGL

Amid rumblings of dissatisfaction—and a few open defections—developers of 3D games are trying to deal with delayed and canceled releases of Microsoft's critical Direct3D API.

Direct3D, part of Microsoft's DirectX APIs, provides a software interface between application programs and 3D accelerators. It includes a hardware abstraction layer (HAL) that translates the commands and data structures into the proper format for the 3D hardware. Direct3D also includes a hardware emulation layer that takes over some functions for 3D accelerator chips that provide only partial acceleration.

Microsoft had planned to release version 3.0 of DirectX in August, but it did not ship until November. A Microsoft developers conference in November was postponed until April. DirectX 4.0 has been canceled entirely, and DirectX 5.0 is not expected until midyear.

Direct3D's immediate mode is the focus of most of the trouble. Application software sends commands to Direct3D in execute buffers that are difficult to manage. Direct3D also suffers from hardware implementation problems. Microsoft has no program in place to test or enforce the compliance of 3D hardware with Direct3D. Some boards claim to implement certain features but actually don't, causing trouble for software developers that try to make use of those features. Direct3D provides capability bits to describe which features are supported, but it's difficult to develop applications that support all possible combinations.

At least one game developer has chosen not to support Direct3D until these problems are fixed. John Carmack, cofounder of Id software and lead programmer for Quake, the company's popular 3D shoot-'em-up, has been vocal in his criticisms (*finger johnc@idsoftware.com*). Describing his effort to port Quake to Direct3D, he writes, "Direct3D Immediate Mode is a horribly broken API." Id canceled its Direct3D effort and now plans to release an OpenGL-based version of Quake.

OpenGL is similar to Direct3D's immediate mode and is said to have a number of advantages, including greater ease of use. Instead of execute buffers, applications simply provide a sequence of subroutine calls, each describing one vertex of a triangle. OpenGL products must pass a set of compliance tests, making performance more predictable. This increases the cost of OpenGL hardware but eliminates the need for Direct3D's capability bits and piecemeal approach to emulation.

The Direct3D controversy may also affect Microsoft's Talisman. The company's original plan was to add extensions to Direct3D to control new Talisman features such as image layers, texture compression, and anisotropic filtering. These extensions are due by the end of 1997, but any substantial changes to the baseline Direct3D API would likely delay these new features and push most Talisman applications into late 1998. Microsoft has also announced plans to add Talisman support to its implementation of OpenGL, covering its bases in the event that more game developers reject Direct3D.

The delays in DirectX releases from Microsoft may signal major changes in Direct3D. Microsoft has often released hastily prepared software just to get a foothold in a new market (probably starting with MS-DOS 1.0) and later followed up with significantly improved code. We hope that will be the case here.

C compiler for MSP's ARM and vector processors, as well as an assembler, linker, and debugger. Samsung added simulator, profiler, and decompiler tools. The tools are available for Windows 95 PCs or SPARC workstations. The lack of C++ support, as in the TriMedia development environment, is not disabling; most driver and codec development will take place at the lower C and assembly-language levels.

No matter who provides the software, all vendors of media processors remain at Microsoft's mercy for the APIs needed to use their processors under Windows. Many uncertainties remain in these software interfaces. For example, a system with an MMX processor and a media processor could perform some multimedia tasks on either chip. Chromatic is developing an x86-based resource manager that could assign a task to the least busy device, but it will be difficult to do this in a Windows-compatible way without Microsoft's help.

Microsoft's Direct3D API is coming under fire from software vendors (see sidebar). Changes in the API would force media-processor vendors to change their software—and possibly their hardware as well, since Direct3D determines the features that 3D accelerators must support.

Product Positioning Open to Debate

These three vendors claim their media processors bring high-end features to the PC market. Chromatic emphasizes Mpact 2's 1M-polygon/s 3D throughput in support of this positioning, for example. By the time Mpact 2 arrives, however, 1M polygons/s will be merely midrange performance; dedicated 3D chips such as the Vsis 3DPro already exceed this mark. Since media processors must be priced at about $50 to meet OEM budgets, it is unrealistic for any of the media-processor vendors to expect to surpass the performance of more expensive 3D-only hardware.

At the same time, the three vendors claim their media processors are also suitable for low-end embedded products. Philips's plans include TM-CE, a TriMedia derivative for

	C-Cube VRP CL-4020	Fujitsu MMA	Mitsubishi D30V	Oak (unannounced)	Rendition Vérité
2D acceleration	n/a	n/a	n/a	n/a	Yes (HW)
3D setup (polys/s)	n/a	n/a	n/a	n/a	150K
3D fill rate (pixels/s)	n/a	n/a	n/a	n/a	25M
MPEG-1 decode	Yes (HW)	Yes (SW)	Yes (SW)	Yes (HW)	No
MPEG-2 decode	No	Yes (SW)	Yes (SW)	Yes (HW)	No
MPEG-1 encode	Yes (HW)	No	No	Yes (HW)	No
Video in	Yes	No	No	No	No
Video out	Yes	No	No	Yes	No
Audio support	No	Yes	Yes	Yes	No
Clock rate	80 MHz	180 MHz	250 MHz	67.5 MHz	50 MHz
Integer ops/cycle	4	6	4	1	2
Peak integer perf	0.32 GOPS	1.08 GOPS	1.0 GOPS	0.07 GOPS	0.1 GOPS
Int width at peak perf	8 bits	16 bits	16 bits	32 bits	32 bits
Local RAM bandwidth	160 Mbyte/s	720 Mbyte/s	n/d	67.5 Mbyte/s	400 Mbyte/s
Price for chip	n/d	n/d	n/d	n/d	$40
Production date	Now	n/d	n/d	n/d	Now

Table 2. Among special-purpose media processors, MMA and D30V offer the highest integer performance, while VRP supports MPEG encoding and Vérité speeds 3D rendering. n/a=not applicable, n/d=not disclosed (Source: vendors)

consumer electronics. Samsung proposes MSP as a good part for video games and set-top boxes, and Chromatic has even suggested using Mpact for multimedia acceleration under Windows CE.

These plans also may be unrealistic. Media processors must be powerful and sophisticated to meet the needs of the PC market, but this requirement burdens them with relatively large die sizes made on advanced fab lines. This burden will make them uncompetitive with parts designed for low-cost applications. Instead, media-processor vendors should focus on the mainstream PC market, at least 40 million units a year—certainly an opportunity worth pursuing, and one that will require their full attention.

C-Cube Concentrates on Video Compression

Chromatic, Philips, and Samsung form the "Big Three" of the media-processor business, but other companies plan to use programmable architectures to good advantage in narrower markets. C-Cube, for example, has been a long-time advocate of programmable engines for digital-video compression and decompression.

C-Cube's VideoRISC processor (VRP) is widely used for MPEG-1 and MPEG-2 encoding by digital satellite TV broadcasters, but VRP derivatives could certainly be adapted to other tasks. The core of VRP is a fairly conventional RISC design. It executes 32-bit integer instructions in a five-stage pipeline and also supports a set of SIMD operations on four byte-size operands in an eight-stage pipe shared with the integer engine.

Like most media processors, VRP includes some fixed-function logic. A variable-length-coding unit offloads the relatively simple data-compression tasks from the CPU, and a motion estimator accelerates MPEG compression by comparing 8×8-pixel blocks against two reference frames at an effective rate of two billion operations per second.

Even with its on-chip caches, DRAM controller, and video and host I/O interfaces, VRP is small enough to allow C-Cube to offer one or two complete VRPs on a single chip. The current implementations run at up to 80 MHz. At this speed, a single device can perform limited MPEG-1 encoding; multiple VRPs in parallel are used for higher quality and for MPEG-2 encoding.

Future VRP derivatives could include more than two VRPs per chip and operate at higher clock rates. Digital video is likely to become a major application segment in the next few years, and with the simple addition of a PCI interface, VRP could become a strong player in that market. Adding support for additional data types, including 2D/3D graphics and audio, could make VRP into a true media processor competitive with Mpact, TriMedia, and MSP. C-Cube's relationships with OEMs like Diamond, Matrox, and Orchid would provide good sales channels for such products.

Fujitsu, Mitsubishi, Oak Seek DVD Role

Fujitsu's multimedia assist (MMA) processor is a relatively simple 32-bit, two-way LIW design with limited 16-bit SIMD support. With a peak throughput of 1.08 BOPS at 180 MHz, the part is capable of DVD decoding but requires a separate SparcLite host processor.

MMA includes a graphics controller, audio interfaces, and several built-in peripherals but lacks a PCI interface, floating-point support, and 3D rendering capabilities. Without these capabilities, MMA is not useful for PC multimedia applications. In the DVD application, however, MMA is a good fit. By way of comparison, MMA could replace as many as seven of the devices found in Toshiba's reference DVD player chip-set design.

Mitsubishi has developed the D30V, a programmable chip intended mainly for consumer devices. At just 37 mm^2, the D30V is the smallest of all announced media processors. At 250 MHz, it is also the fastest, as Table 2 shows. The high clock speed allows the chip to use a simple two-way LIW architecture very similar to MMA's. Even with its small die, the D30V includes 64K of on-chip memory split between instruction and data storage. The D30V also includes audio and video output circuitry and a variable-length decoder.

Oak Technology is considering its options in the DVD market. While Oak has not yet announced any parts, the company provided a fairly specific description of a RISC-based DVD decoder at the 1996 Microprocessor Forum.

The design includes a 32-bit RISC engine, but hardwired function units handle most of the work. MPEG-2 and

AC-3 decoders are included, with the RISC core managing the flow of data within the device and its local memory. Such a part strains the definition of a media processor, but the presence of a programmable engine would make it easier to add additional features should Oak develop an interest in other markets.

These vendors may be satisfied with the DVD market—a total of several million units by 1998—but media processors designed for DVD could provide a foundation for future media processors for the PC market.

Rendition Remains Focused on 3D Graphics

Rendition's Vérité V1000 has become one of the more successful 3D accelerators in the PC 3D market. This is due in large part to Rendition's ability to form strategic relationships within the PC industry.

The V1000 is not a multimedia processor and provides only average 3D acceleration, but the part's programmability makes it more flexible than its competitors in the 3D-accelerator market. The core of the V1000 is a 32-bit RISC processor with limited VLIW capabilities. The CPU core handles 3D setup and some 2D acceleration functions. With no floating-point capability of its own, the V1000 depends on host-based geometry processing. Rendition has used this programmability to implement custom antialiasing algorithms and special effects for game titles.

The part is used in graphics adapters from Canopus, Creative Labs, Intergraph, and Number Nine, and at least 19 software vendors have announced support or, in most cases, actual products. The V1000 is currently the only 3D accelerator supported by Quake, a distinction other 3D chip vendors must envy. Rendition has not announced a successor to the V1000, but we expect to see one early this year, offering more competitive performance and reinforcing Rendition's solid position in the market.

Missing in Action: Mfast, MicroUnity, and Nvidia

In spite of impressive specifications, IBM's Mfast project has been canceled. First described at the Microprocessor Forum in 1995, Mfast was designed to yield 10 BOPS of sustained performance on 16-bit operands and was planned to ship in mid-1997. Research continues, but all product plans have been shelved.

MicroUnity's original MediaProcessor, an impressive five-thread 1-GHz BiCMOS design, failed for lack of applications requiring its level of performance (and able to pay its price), but the company continues to develop a single-threaded CMOS MediaProcessor that may find uses in cable modems or other broadband-RF devices.

Nvidia's NV1 became a casualty of mixed messages. While it is an adequate 3D accelerator that offers audio support through an integrated DSP engine, the chip's sales suffered from a mistargeted and misunderstood marketing campaign touting its nonstandard 3D interface. Today, the NV1 is essentially obsolete. The NV3, planned for a 1Q97 debut, will drop audio support and programmability in favor of pure 3D performance for Direct3D. SGS-Thomson manufactured the NV1, and we expect it will also make the NV3 despite the company's involvement with Chromatic.

Multimedia Milestones of 1996

Chromatic *(www.chromatic.com)* began shipments of its Mpact 1 media processor and disclosed the design of its next-generation Mpact 2 device (11/18/96, p. 1). The company later said SGS-Thomson will join LG Semicon and Toshiba in building and selling Mpact chips (12/9/96, p. 5).

Fujitsu *(www.fujitsumicro.com)* debuted its MMA design, a media processor intended for DVD players (11/18/96, p. 11).

MicroUnity *(www.microunity.com)* canceled its BiCMOS media processor, laying off much of its staff (8/5/96, p. 5). The company is developing a simpler CMOS processor for cable modems (10/28/96, p. 4).

Mitsubishi *(www.mitsubishi.com)* developed the D30V, a single-chip DVD decoder (12/9/96, p. 1).

Oak *(www.oaktech.com)* previewed a DVD decoder with a programmable RISC core (11/18/96, p. 5).

Philips *(www.semiconductors.philips.com)* neared completion of its TM-1 media processor.

Rendition *(www.rendition.com)* rolled out its Vérité chip, a programmable 3D accelerator (5/6/96, p. 1).

Samsung *(www.ssi.samsung.com)* introduced its media processor, dubbed MSP and expected to ship in 3Q97 (8/26/96, p. 1).

Intel's **AGP** interface *(www.teleport.com/~agfxport)* is expected to become a standard for high-bandwidth 3D graphics accelerators (6/17/96, p. 11).

Microsoft announced **Talisman** *(www.microsoft.com/hwdev/devdes/talisman.htm)*, aimed at providing high-performance 3D for future PCs (8/26/96, p. 5).

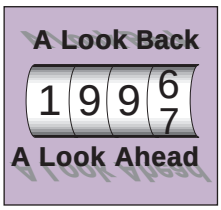
Media-Processor Market Maturing Rapidly

Chromatic and Philips have spent years preparing for success in the PC market, and this year they will have their chance. Media processors from these two vendors should appear in many systems during the 1997 holiday buying season. By this time next year, the two vendors will have moved on to second-generation cores while Samsung and others will be firing their first shots in the PC market. Vendors such as Fujitsu and Mitsubishi are saving their ammunition for the consumer market, where they will compete mainly against fixed-function devices.

Two years ago, programmable multimedia engines were virtually unheard of. As recently as last year, the viability of the concept was still in doubt—could programmable devices really compete with hardwired logic? Today, we can answer in the affirmative. MR

Embedded Vendors Seek Differentiation

Signal Processing, Code Compression, ASIC Cores Enable Specialization



by Jim Turley

The past year saw unit sales of every major 32-bit embedded microprocessor family grow, some by dramatic leaps. In 1996, 32-bit volume reached nearly 120 million units, a healthy 15% increase over the previous year. SuperH and MIPS tangled for top RISC honors, while 68K retained the 32-bit crown. Advanced RISC Machines, MIPS, and PowerPC grew the fastest, with ARM volume doubling, MIPS growing 3×, and embedded PowerPC sales increasing five-fold. These enviable increases were due largely to the success of moderately priced consumer-electronics items. The past year also saw many vendors begin to differentiate their parts through a number of technological or marketing approaches.

Hitachi jumped on the DSP bandwagon, MIPS sprung for code compression, ARM did both, and PowerPC did neither. Many embedded microprocessors made evolutionary moves toward more real-world signal or media processing—some more than others. The coming year should see MIPS' wild ride continue, PowerPC gain ground, and a product-strategy turnaround for Intel's i960 family.

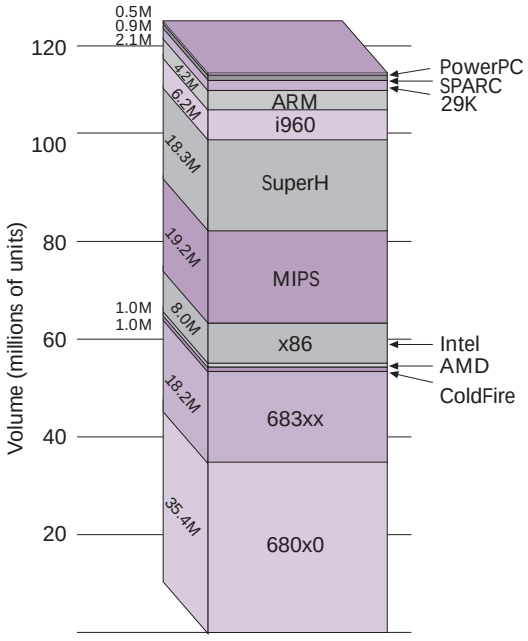


Figure 1. As in previous years, Motorola's 68K family led in embedded 32-bit shipments. MIPS chips and Hitachi's SuperH line both enjoyed huge sales in 1996, due largely to popular game consoles. Ironically, AMD's moribund 29K products enjoyed their best year yet, with 2.1 million units. (Source: MDR)

Voltage and Power Drop, DSP Gains Ground

IC processes moved ahead one generation: all the leading embedded CPUs are now built in 0.35-micron (drawn) processes. Power supplies are routinely pegged at 3.3 V, and several parts debuted in 1996 with supply voltages well below that level. Pico-power processors running at 2.5 V, 2.2 V, and even 1.65 V now set the pace in the power/performance race.

High-end 32-bit performance can now be had for under 500 mW, once the domain of 16-bitters. The market for low-power devices is emphasizing fab technology more than embedded chips have done in the past. The vendors are now bifurcating: some use older fab lines to minimize cost; others use leading processes for the best power/performance.

Other trends were less predictable. Digital signal processing has taken on a whole new importance in the marketplace as cellular telephones, pagers, electronic organizers, and PDAs proliferate. All these applications call for strong signal-processing performance combined with small physical size and moderate power consumption. The solutions were as varied as they were unusual.

The easiest approach, and the one taken by most vendors, was to add a simple multiply-accumulate (MAC) instruction to their standard instruction sets. Some vendors (IDT, Hitachi, and others) back up the new MAC instruction with specialized hardware, while others simply rely on the existing multiply unit. The MAC helps with inner-loop filtering algorithms, but a MAC unit does not a DSP make.

Taking things a step further were Hitachi and ARM, both of which added full-on DSP engines to their CPUs. Although differing in the details, both SH-DSP and Piccolo add several new DSP-only instructions that execute on specialized DSP hardware. Remarkably, both approaches maintain binary compatibility with previous versions of the architecture. They come much closer to many customers' ideal of a merged digital signal processor and microcontroller.

Most such signal processing today is for data transmission, either wireless (as in a digital cell phone) or cabled (software modem), in part because that's what low-cost DSP chips and host-based CPU/DSP hybrids are capable of. As signal-processing capabilities improve, more will be asked of these devices. Noise cancellation, speech recognition, image recognition, and image compression and decompression will be among the new features added as these appliances evolve.

The trend toward integrated signal processing will continue unabated through 1997 as existing vendors heap more DSP capability onto their architectures, sacrificing varying amounts of backward compatibility for DSP performance. A few new architectures will also debut—hybrids designed especially with control-oriented signal processing in mind.

Code Compaction Coming On Line

Another trend evinced in the year's events was the press toward code compaction. Following on the heels of ARM's Thumb, MIPS introduced MIPS-16, a similar approach to compressing 32-bit instructions into 16-bit words. Thumb has already begun showing up in products; chips equipped with the MIPS-16 predecoder should roll out by mid-1997.

Code compaction is an important issue for many embedded system designers. Most are willing to sacrifice some performance—as both Thumb and MIPS-16 must—to reduce memory costs. The wise and sagacious designers of the x86 and 68K instruction sets don't have this problem; their code was designed to be compact from the outset. It is the RISC-descended chips that must now deal with code bloat. PowerPC, SPARC, and the i960 are the next obvious candidates for code-compression alterations.

Volume Picks Up—for Some More Than Others

As Figure 1 shows, the big 32-bit volume winner for 1996 was the same as for every previous year: Motorola's 68K. Particularly in embedded markets, the older architectures such as the 68K and the x86 have the advantage of more design-ins. The newer RISC chips, however, enjoy higher growth rates.

The big RISC winners in 1996 were MIPS and Hitachi's SuperH, nearly neck-and-neck with 18–19 million units apiece. The i960, PowerPC, ARM, and the 29K were but distant competitors. Except for PowerPC, in no event were computer-system shipments even remotely responsible for the success of the RISCs. SuperH, i960, ARM, and 29K are entirely embedded, and even MIPS owes better than 90% of its volume to embedded applications. Only PowerPC owes its success to computers, with roughly 90% of PowerPC chips going into Macintoshes.

This year, MIPS and SuperH paralleled the perennial sales battle between the Ford Taurus and the Honda Accord. Like Ford, MIPS appears to have out-shipped its Japanese competitor by a nose this year. (By the time this issue went to press, MIPS could account for 17.2 million units, with another 2 million "probable," based on Nintendo figures.) The company also likes to point out that all MIPS processors are 32-bit chips, implying some 16-bit contamination from the low end of its competitor's SH-1 chips. MIPS not only looks to be in the top RISC spot but is enjoying rapid compounded growth, two attributes rarely seen together.

Perennial Standards Hold Their Positions

Intel and AMD continued, of course, to milk the x86 cash cow. These fully amortized, well-supported chips are risk-free, lucrative business for both companies, steadily filling their fab lines long after the design cycle is over. Money for nothing, and the chips are free.

As in previous years, Intel did nothing to its former PC processors other than change their prices and the organization responsible for their marketing. They remain the standard against which all others compare favorably.

AMD differentiated its chips with faster clock rates, lower power consumption, or different on-chip I/O. AMD added a 486 core to its integrated Elan family and gave up trying to sell its 486DX5-133 (*née* 5x86-P75) into desktops as a Pentium placebo. The company's 1.0 million units for 1996—less than half of its 29K volume!—reflects the youthfulness of its 32-bit offerings. Elan has been shipping all year, but the Elan 310 debuted in April, and the 486 Elan didn't start production until 3Q96. AMD's 1.0 million embedded x86 shipments did not significantly add to—or subtract from—the company's $69 million loss in 1996.

	NEC R4300	IDT RV4640	National 486SXL	Intel 960JA	Intel 960HT	Motorola 68EC040	Motorola 68EC060	AMD 29040	Motorola 860DC
Architecture	MIPS	MIPS	x86	i960	i960	68K	68K	29K	PowerPC
Clock rate	**133 MHz**	**133 MHz**	25 MHz	33 MHz	60 MHz	40 MHz	66 MHz	50 MHz	40 MHz
I/D cache	**16K/8K**	8K/8K	1K	2K/1K	**16K/8K**	4K/4K	8K/8K	8K/4K	4K/4K
FPU?	Yes	Yes	No	No	No	No	No	No	No
MMU?	Yes	Yes	No	No	No	No	No	Yes	Yes
Bus width	32 bits	32 bits	16 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
Bus frequency	**66 MHz**	44 MHz	25 MHz	33 MHz	20 MHz	40 MHz	33 MHz	25 MHz	40 MHz
MIPS	160 MIPS*	**175 MIPS**	12 MIPS	28 MIPS	100 MIPS*	44 MIPS	101 MIPS	67 MIPS	52 MIPS
Voltage	3.3 V	3.3 V	5 V	3.3 V	3.3 V	5 V	3.3 V	3.3 V	3.3 V
Power (typ)	2.2 W	2.1 W	0.6 W	0.5 W	4.5 W	4.5 W	n/a	1.0 W	0.9 W
MIPS/watt	73	**83**	20	56	22	10	n/a	67	58
MIPS/dollar	**5.00**	4.17	0.8	0.76	0.79	0.59	0.18	0.78	1.24
Transistors	1,700,000	1,050,000	350,000*	750,000	2,300,000	1,170,000	2,530,000	1,200,000	1,800,000
IC process	0.35µ 3M	0.6µ 3M	0.65µ 3M	0.8µ 3M	0.6µ 4M	0.65µ 3M	0.5µ 3M	0.35µ 3M	0.5µ 3M
Die size	45 mm²	56 mm²	n/a	64 mm²	100 mm²	163 mm²	217 mm²	61 mm²	25 mm²
Est mfg cost*	$11	$15	$8	$8	$34	$30	$55	$20	$20
Availability	Now	Now	Now	Now	Now	Now	Now	Now	Now
Price (10K)	$32	$42	$15	$37	$126	$75	$180	$86	$42

Table 1. Among processors for embedded applications, MIPS processors from NEC and IDT offer the best performance, along with Digital's StrongArm processor. Older processors such as Intel's i960 and Motorola's 680x0 can't match the price/performance of these speedy new RISC processors. n/a indicates information not available (Source: vendors except *MDR estimates)

The coming year should hold as few surprises as the last regarding embedded x86 announcements. Neither firm is quite ready to relegate Pentium or K5 to the embedded market. Intel has been publicizing a few embedded Pentium design wins but, like embedded Alpha chips, the volumes are negligible. As desktop systems devour the fastest chips, it's inevitable that low-end Pentiums will find their way, unchanged, into the embedded arena.

Once desktop penetration of AMD's K6 picks up later this year, the original K5 core may start to go the way of the 386 and 486 cores before it. However, even a cursory analysis of the economics points out that the K5 is not the most cost-effective route to higher performance. The K6, with virtually the same die size as the K5, may make a better basis for a series of embedded processors.

A number of new companies offering x86-compatible parts for desktop or embedded systems should also spring up in 1997. One early entry was Acer, which merged its 386SX clone with its existing core-logic chip set. Two companies, Texas Instruments and UMC, called it quits in 1996 and exited the x86 business.

Motorola continued apace with its 680x0, 683xx, and ColdFire families. Toward the end of the year, a twitch of life came from the stalwart 680x0 line in the form of a 66-MHz upgrade to the 68EC060 and a steep price discount on the 50-MHz chip (see Table 2). The company also laid out its plans for the midrange ColdFire line, promising regular performance upgrades that should pace the industry average.

Motorola will continue to push ColdFire as its embedded architecture of choice, maintaining the 680x0 chips for the sentimental and the PowerPC line for RISC fans. As in previous years, integrated logic and peripheral I/O will be Motorola's key differentiating factors.

Intel had a very quiet 1996 in both its desktop and embedded product lines. The good ship i960 is still coming hard about, turning away from the standalone microprocessor business and steering a course toward more integrated designs. Following the release of the i960RP, a fleet of faster and newly integrated i960 parts should dot the landscape in 1997. All of them will, in some form or other, aid and abet sales of Intel-based systems. Printer controllers, storage controllers, and I/O processors are likely at the first launch.

MIPS Plays Its Way Into the Lead

Despite a mixed financial year for parent company Silicon Graphics, 1996 brought reason for celebration in the halls at MIPS Technologies. Shipments of MIPS-based processors shot up somewhere beyond 17 million units (the company's licensees have not completed their tally), more than triple the previous year's shipments, which were more than triple the volume of the year before that.

The spectacular volume growth in MIPS chips was due in large part to two Japanese giants, Sony and Nintendo. Together, these companies accounted for almost half of the MIPS volume. Sizable shipments were also allotted to makers of printers and network equipment such as Cisco, Oki, and QMS. The MIPS cash register rings twice for each Nintendo 64 game player: once for the R4300 CPU and then again for the R3000-based graphics chip. Even without the game platforms, MIPS shipped more units than either the i960 or ARM.

The coming year should be bountiful, too, though MIPS is not projecting another 200% growth spurt. More page printers sporting R4300-derived processors will appear in 1997, and more networking vendors like Bay and Cisco will ramp production of their MIPS-based units. Sales of the Sony and Nintendo units are also likely to grow.

	SA-110	ARM710	SH7604	PPC 401GF	R4100	960SA	CF5102	486SXSF	29040
Vendor	Digital	VLSI	Hitachi	IBM	NEC	Intel	Motorola	Intel	AMD
Clock rate	**200 MHz**	40 MHz	20 MHz	50 MHz	40 MHz	20 MHz	25 MHz	33 MHz	50 MHz
I/D cache	**16K/16K**	8K	4K	2K/1K	2K/1K	512/0K	2K/1K	8K	8K/4K
FPU?	No	No	No	No	No	No	No	No	No
MMU?	Yes	Yes	No	No	Yes	No	No	Yes	Yes
Bus width	32 bits	32 bits	32 bits	32 bits	32 bits	16 bits	32 bits	32 bits	32 bits
Bus frequency	**66 MHz**	40 MHz	20 MHz	50 MHz	20 MHz	20 MHz	25 MHz	33 MHz	25 MHz
MIPS	**230 MIPS**	36 MIPS	20 MIPS	52 MIPS	40 MIPS*	9 MIPS	27 MIPS	16 MIPS*	67 MIPS
Voltage §	2.0/3.3 V	5 V	3.3 V	3.3 V	3.3 V	5 V	3.3 V	2.7/3.3 V	3.3 V
Power (typ)	900 mW	424 mW	200 mW	140 mW	**120 mW**	1,100 mW	900 mW	515 mW	1,000 mW
MIPS/watt	239	85	100	**371**	333	8	30	31	67
MIPS/mm²	**4.30**	1.04	0.24	2.36	1.60	0.17	n/a	n/a	1.63
Transistors	2,100,000	570,295	450,000	300,000*	450,000	346,000	n/a	n/a	1,200,000
IC process	0.35µ 3M	0.6µ 2M	0.8µ 2M	0.5µ 3M	0.5µ 3M	1.0µ 2M	0.6µ 3M	0.8µ 2M	0.35µ 3M
Die size	50 mm²	34 mm²	82 mm²	22 mm²	25 mm²	51 mm²	n/a	n/a	41 mm²
Est mfg cost	$18*	$9*	$7*	$4*	$8*	$4*	$9*	$15*	$20*
Availability	2Q96	Now	Now	Now	Now	Now	Now	2Q96	Now
Price (10K)	$49	$28	$27	$13	$25‡	$13	$25*	$72†	$86

Table 2. Among processors aimed at portable devices, Digital's StrongArm offers by far the best performance. The R4100 ranks among the fastest processors in this table while sipping just 120 mW. The PowerPC 401GF offers excellent performance at a low list price. †list price in 1,000s ‡list price in 100,000s §core/bus voltage n/a indicates information not available (Source: vendors except *MDR estimates)

The new crop of handheld PCs running Windows CE will also push MIPS up a bit through 1997. Two of the six HPCs announced last fall use MIPS processors; in addition, General Magic has finished porting its Magic Cap OS to MIPS and may soon enter the market with a unit of its own. Moving from the palmtop to the set top, Philips and Sony (both MIPS licensees) are peddling WebTV, based on IDT's R4650. A growing number of cable and satellite decoders also rely on MIPS processors.

ARM Touches Power-Sensitive Designers

ARM had another banner year, more than doubling its volume to about 3.4 million ARM-based ASICs and another 800,000 standalone ARM chips like the 610, 710, and 7500. The biggest consumers of ARM, by far, were makers of portable, battery-powered equipment: digital cellular telephones, pagers, and PDAs.

Cell phones account for the largest proportion of low-power designs. Sales of most PDAs (ARM-based or otherwise) are sluggish. Most pagers today don't need the capabilities of a 32-bit microprocessor, but the company expects a spate of new ARM-based pagers to hit the market in 1997.

The ranks of the ARM licensees swelled to 17, with Rockwell officially signing on just after the first of the year. The list of semiconductor companies not holding ARM licenses keeps shrinking, seemingly limited to just Intel and Motorola—for now. What with ARM's penetration into the cellular, paging, and portable computing markets, it seems probable that one of these two holdouts may soon fall in line.

ARM chips and cores also made inroads into network computers and set-top boxes, like the ones from Teknema, Wyse, and Boundless (*née* Sun River), and into some truly embedded uses like modems. The volume leader for ARM, in fact, is Cirrus Logic's CL-MD34xx modem-chip family.

ARM rightly understands its microprocessor cores are generally not the most interesting feature of its customers' products. That is, ARM cores are not differentiators, they're enablers. Except for a single high-profile design win (Apple's Newton), the company is doomed to succeed in obscurity.

In 1996, ARM rolled out a pair of technological innovations, and its development work on Thumb started to pay off. The Thumb code-compression circuit is shipping in set-top decoders and automotive controllers from TI and in a number of unannounced digital cell-phone chips.

StrongArm—a small microprocessor cunningly concealed inside a large cache—gave a much-needed performance boost to the ARM product line early in 1996, as Table 2 shows. It was a feather in ARM's cap and gave a welcome, albeit modest, financial boost to codesigner Digital.

It's hard to say whether ARM needed Digital more than Digital needed ARM, but both companies benefited from the arrangement. ARM gained a much-needed boost to its high end and maintained its design win with Apple. For its part, Digital gained a relatively high volume (compared with Alpha) part to fill its expensive fab lines.

Key Embedded Events of 1996

SGS-Thomson offered its 120-MHz 486DX4 core as an ASIC cell (1/22/96, p. 13), while UMC exited the x86 business under legal pressure from Intel (1/22/96, p. 13).

AMD moved its 486DX5-133 into the embedded market (10/7/96, p. 4) and expanded the Elan family with a less-expensive SC310 (4/15/96, p. 4) and a 486 core (10/28/96, p. 4).

Digital's SA-110 StrongArm chip debuted at 200 MHz (2/12/96, p. 1), then got a quick upgrade to 233 MHz (10/7/96, p. 4).

Mitsubishi unveiled an innovative device combining DRAM and a CPU (5/27/96, p. 10), which it licensed to Motorola in exchange for the ColdFire and 68EC000 cores (10/28/96, p. 4).

Embedded **PowerPC** ranks were swelled at the low end by IBM's 401GF (6/17/96, p. 9) and Motorola's 801 (8/26/96, p. 4). Motorola also developed the PowerPC 823 chip for digital cameras (5/27/96, p. 4).

Argonaut RISC Cores (ARC) began licensing its synthesizable CPU core (7/8/96, p. 8) and signed Brooktree as its first licensee.

IBM signed a remarketing agreement with Mitsubishi for embedded PowerPC processors (8/5/96, p. 5) and Hitachi gave VLSI the nod for ASIC development with the SuperH core (8/26/96, p. 4).

ARM's Piccolo DSP module promised to add signal-processing capability to ARM cores (11/18/96, p. 17).

Sun detailed its PicoJava CPU core, designed to run Java bytecodes natively (10/28/96, p. 28) and signed four licensees (6/17/96, p. 4).

Hitachi's SH-4 added superscalar execution and a 288-bit floating-point unit for graphics manipulation (10/28/96, p. 32).

MIPS worked up MIPS-16, a compressed, 16-bit form of the MIPS instruction set (10/28/96, p. 40) and the MDMX multimedia extensions.

Philips produced three derivatives of its Toshiba R3900-derived chip set: the 31500 (10/7/96, p. 4), the 31100 (9/16/96, p. 4), and the 30100 (1/22/96, p. 4).

Motorola laid out its roadmap for ColdFire enhancements for the next five years (9/16/96, p. 1).

Diba hooked up with Zenith, NEC, and Mitsubishi for its Internet-appliance technology (8/26/96, p. 19).

Windows CE debuted with support for five microprocessor architectures: x86, MIPS, SuperH, PowerPC, and ARM (12/30/95, p. 4 and 9/16/96, p. 4).

Apple stuck with ARM for StrongArm-based Newton 2000 (11/18/96, p. 4); Motorola canned 68K-based Marco and Envoy PDAs (12/30/95, p. 4), while General Magic eschewed 68K for MIPS with revamped Rosemary (12/30/96, p. 4).

The drawback is that StrongArm is currently a point product that breaks the tradition of giving customers a modular, a la carte, CPU core to embed into custom logic. Digital has no ASIC expertise and, at least for now, StrongArm is not being fabricated by any vendor that has. As impressive as the SA-110 is, it doesn't fully further the goals of ARM or address the needs of its customers.

What's needed is a portable core with more performance than ARM7 can offer. The company has promised to deliver just those characteristics with the ARM8 and ARM9 cores, but neither chip has fulfilled those goals. The ARM8's *raison d'être* is its wide, double-clocked cache interface (see MPR 12/25/95, p. 4), which is too finely tuned for ASIC integration. The core appears only in VLSI's ARM810 chip, which seems destined for Acorn systems or something like a low-end Newton.

The ARM9 core, on the other hand, should be more portable and less vendor-specific, positioning it as the modular upgrade from ARM7. Though already licensed, ARM9-based parts are not due to tape out until 3Q97, meaning production is more than a year away.

Digital is addressing some of the need for embedded StrongArm cores by readying a collection of application-specific StrongArm derivatives. Due to roll out in 1997, these chips should be a good fit for PDAs, set-top boxes, and games.

PowerPC Still Building Up Steam

PowerPC is the only product line except x86 that owes a significant share of its volume to computer sales. Only about 500,000 PowerPC chips went into embedded applications—far fewer than even the 29K and on a par with SPARC. On the plus side, that number is about five times what it was in 1995.

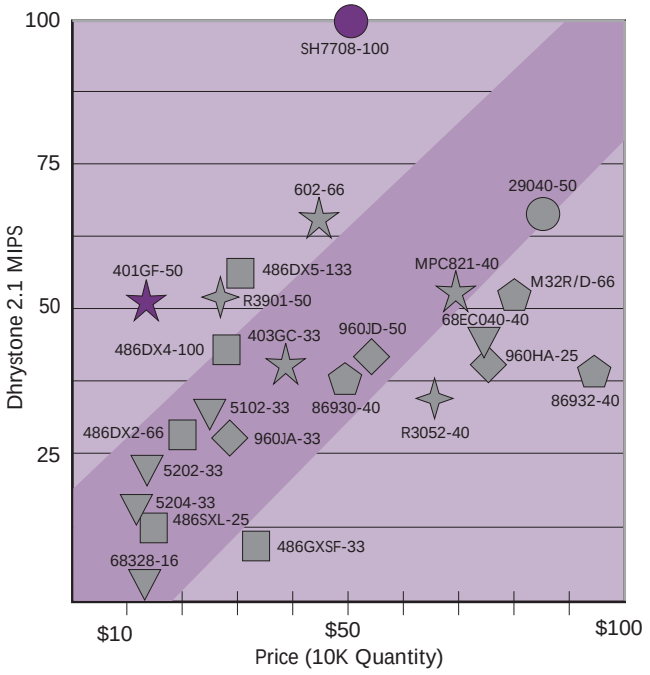


Figure 2. A few chips, like IBM's 401GF and Hitachi's SH7708, are off the usual curve for price/performance. (Source: vendors)

Considering the combined marketing and manufacturing muscle behind PowerPC, it's disappointing—but not particularly surprising—that the architecture has not made a better showing. Outside of a market where compatibility with installed software is vital, PowerPC chips have offered very little to recommend themselves. As a group, they excel neither in power consumption, code density, price, nor performance. Only IBM's 401GF, shown in Figure 2, can mount a credible assault on the leading embedded RISC chips.

Motorola and IBM continue to pursue somewhat different strategies in the embedded market: Motorola emphasizing its broad intelligent I/O library as IBM pushes customer-driven designs while its own organization comes up to speed. IBM has had success in television appliances, with set-top boxes from RCA (Thomson), Tatung, NEC, and Acer accounting for much of its volume. Both companies have found the perception of Macintosh compatibility to be a double-edged sword; it helps sell embedded chips only so long as Apple's fortunes are rising.

With Apple's purchase of Next and the promised replacement of Mac OS, the Mac's future has never been more in doubt (see page 3). If Apple continues to falter, embedded customers may quickly rethink their priorities. To succeed in the embedded marketplace, PowerPC must show it can stand on its own merits. IBM's 401GF is an excellent move in that direction: a fast performer with modest power consumption and an exceptionally low price. Throughout 1997, IBM will leverage the 401's core to produce more application-specific derivatives.

PDA Scene About to Change in 1997

With Microsoft's much-ballyhooed release of Windows CE, the company finally gave serious attention to alternative CPU architectures. After the initial MIPS and SuperH ports, the company added x86, PowerPC, and ARM (including StrongArm), covering just about all the important bases.

Although by some estimates, Apple has shipped fewer than 125,000 Newtons in that product's entire life span, the new Newton 2000 (N2K) may redeem both Apple's and ARM's faith in the platform. With 8–10 times the integer performance of earlier Newtons, the N2K may actually live up to users' expectations. With a retail price of about $1,000, though, the N2K is twice the price of most WinCE units, which are themselves twice the price of U.S. Robotics' popular Palm Pilot (a 68328 design). This price crosses the line from impulse consumer purchase to corporate capital investment and approaches the price of some Macintoshes.

Network Computing Threatens to Open Market

The concept of network computers (slim clients, NCs, NetPCs, PCTV, et al) gripped the popular media during 1996. Left and right, companies rolled out plans both desperate and cunning to break the hold of Intel or Microsoft on the

PC industry. Many strategies were purely ego driven, many were vengeful, some were simply optimism-stoked greed. Adding to the furor was the hype surrounding Java in all its many incarnations. Java gained notoriety as a language, a distribution medium, an operating system, a religion.

As a language, Java has gained adherents who appreciate the discipline it enforces. As an architecturally neutral distribution format, Java has shown its promiscuity, if not its value, with several Web browsers running on any number of computers and operating systems. Java's major advantage is that it runs equally poorly on all microprocessors.

Sun set out to change that situation with PicoJava, a new core announced at the most recent Microprocessor Forum. Sun and its four licensees expect to produce PicoJava-based chips before the end of 1997. While it's not clear that these chips will enhance Java performance much, the devices they're based on should help promulgate Java bytecode distribution.

Sun is more interested in the success of Java than of Java chips, so JIT compilers and interpreters will continue to flourish. As with Windows CE, Java represents an opportunity for embedded microprocessors to serve a general-purpose role. The coming year will prove how eager the world is for Java-enabled devices.

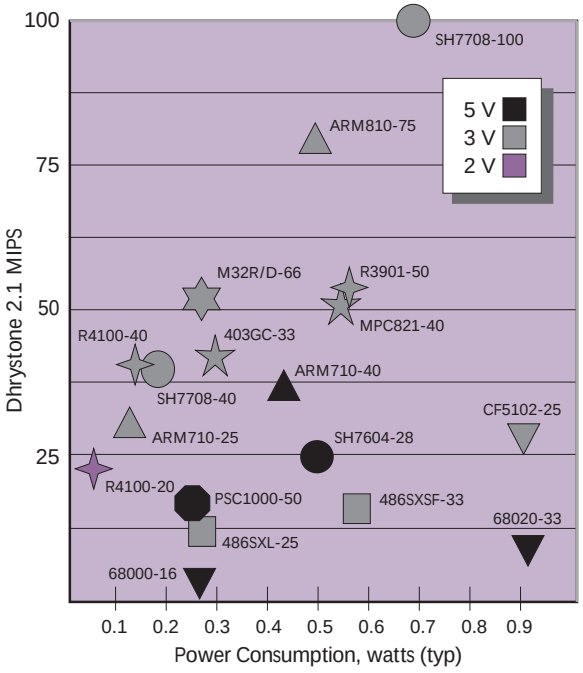


Figure 3. Advances in process technology have yielded a bumper crop of 32-bit embedded chips that consume well under 1 W.

Strange New CPUs Appear

One of the strangest devices to appear in 1996 was Mitsubishi's M32R/D, a combination 32-bit microprocessor and 16-Mbit synchronous DRAM. The oddball part is already slated to appear in Mitsubishi's consumer-oriented Web-access device, based on a Diba design.

Motorola's interest in Mitsubishi's hybrid CPU/DRAM technology prompted the companies to swap recipes late in the year. The technique makes for a powerful combination that should become far more popular in the coming year or two. The advantages in power consumption, board space, access time, and cost are all compelling. Motorola especially, with its corporate emphasis on wireless communications, should benefit from this new technology. Other companies likely to follow suit are those with large DRAM investments and one or more embedded CPU lines, such as Hitachi, Toshiba, and NEC.

Hitachi's SH-4, announced at the most recent Microprocessor Forum, takes graphics processing out on a long limb. It serves its single-minded purpose of radically boosting SuperH graphics performance with a floating-point unit of Frankensteinian complexity. First silicon is due in June; coupled with a Windows CE port, the SH-4 could start appearing in very high end video-enabled consumer devices by the end of this year.

Bracing For More Change in 1997

The vendors of embedded microprocessors are separating themselves into two camps: those that pursue innovative architectural extensions and those that stay the course. The former also tend to be the ones pushing process technology and emphasizing low power consumption. NEC, LSI Logic, Hitachi, and Digital are examples of the former; Intel, AMD, and Motorola are in the latter camp.

Digital's SA-110 chip, Hitachi's SH-4 design, and Mitsubishi's M32R/D are all hallmark devices, signposts marking turning points in the 32-bit embedded roadmap. They all innovate in one or more ways, merging outside-the-box design with best-in-class manufacturing.

Even more nonstandard or nontraditional CPU designs are inevitable: instruction sets that are tailored for DVD, MPEG, compression/decompression, audio, or video processing. As it is, entertainment systems are driving specialized CPU development because the market is there. Nintendo sold more game players in the past three months than Sun sold workstations all last year. This volume will determine design goals for the next generation.

With consumer-electronics items driving microprocessor development in many cases, it's inevitable that microprocessors will change. Established ideas about control flow and data types are being turned on their heads. The demands of digital signal processing, code density, and 3D geometry setup are not the things generally taught in Computer Science 101. Yet these are the issues that will determine success or failure for many microprocessors in the coming years.

As new markets and applications appear, the opportunities for microprocessor vendors will improve. Far from forcing a shakeout, the number of microprocessors should increase, although as the technology evolves, it may become harder to recognize them as microprocessors. M

Controllers Proliferate as USB Catches On

Most Controllers Use 8051; Plethora of Nonprogrammable Chips Debut, Too

by Jim Turley

The number of peripheral controllers available for the Universal Serial Bus (USB) has grown dramatically in the past few months, advancing prophecies of USB's eventual ubiquity. Starting from Intel's lone 8-bit microcontroller, there are now a dozen different chips from as many vendors.

Prices for this new crop of USB chips are generally $5–$7, which is only a small price premium over equivalent processors without USB. A handful of special-purpose, nonprogrammable controllers for keyboards are even cheaper, leading a number of PC peripheral OEMs to bring out their first USB-compatible keyboard, scanner, or mouse.

Software support from Microsoft for USB still lags, but peripheral OEMs have worked around Windows' present shortcomings by providing their own drivers. Apart from Intel's chips, all the chip vendors have embraced the Open Host Controller Interface (OHCI) model, guaranteeing register-level compatibility among vendors.

Intel Expands Across the Board

Intel started at the host and worked outward. The company's first USB host controller for PCs debuted early in 1996 with the 430VX/HX chip set for Pentium systems (see MPR 2/12/96, p. 5). Starting with the 430VX/HX, all Intel chip sets include a USB host controller as a matter of course.

Intel's 82930Ax (see MPR 3/5/96, p. 10) was the first CPU with USB and stands as the most popular USB controller in the first wave of peripherals. Based on Intel's 251, a 16-bit upgrade of the paleolithic 8051, the '930A controls peripherals attached as "leaf nodes" in the USB topology.

With the host and end points covered, Intel moved to the middle with a hub chip. The new '930Hx is similar to the '930Ax but adds the capability to act as a USB hub, distributing power and data to three downstream USB ports. The '930Hx is priced at $7, a $1 premium over the '930Ax.

Intel, Opti, and VIA, among others, include USB in their core-logic chip sets, guaranteeing a USB host controller in virtually all PC motherboards by mid-1997. For the upgrade market, CMD Technology offers the 0670, a PCI-to-USB converter that acts as a host controller. The chip, which is also available on a PCI plug-in board, allows retrofitting existing systems for USB support.

Hub Controllers a Popular Target

Philips, Texas Instruments, Thesys, and MultiVideo Labs have all targeted the hub-and-peripheral combination as a potentially lucrative part of the market. With Intel dominating host controllers (i.e., core-logic chip sets) and with leaf controllers too cheap, intermediate hub controllers have the best chance of generating significant revenue.

Philips's hub device, the PDIUSBH11, offers four downstream USB ports, one more than Intel's, as Table 1 shows. Without an internal microprocessor to drive it, the 'H11 relies on a serial-interface engine (SIE) macrocell distributed by Intel and used on both the '930Ax and '930Hx processors. Unlike the '930Hx, the 'H11 includes an extra "internal" port, which is brought out as an I^2C interface. A separate microcontroller can then communicate over USB via this interface.

The Philips approach is a popular one, also appearing on devices from TI and German vendor Thesys. The Thesys hub, dubbed TH6502, has only two downstream ports in addition to its internal port, and it relies on an external microcontroller for intelligence. The internal port appears as an 8-bit parallel interface with generic control signals that work with most microcontrollers.

TI's two hub chips, the TUSB2040 and TUSB2070, are similar to the Philips and Thesys devices. Based on the same SIE logic Philips and Intel use, these chips have four ('2040) or seven ('2070) downstream USB ports. Neither one has an internal microcontroller or even an internal USB port.

An internal port allows the hub chip to control the peripheral in which it is located. Unlike the Intel, Philips, and Thesys parts, the TI chips must use one of their downstream ports for local control. Alternatively, the '2040 and '2070 can be used in standalone USB hub products, unattached to any PC peripheral. CATC (*www.catc.com*) makes such a box, a four-port hub based on its own hub controller.

MultiVideo Labs' W82C620 chip is another nonprogrammable hub controller with four downstream ports and an internal port. The fabless semiconductor company has plans for a future intelligent version based on an 8051 core, similar to Intel's '930Hx.

Part	8x930Hx	H11	TH6502	2040	2070	W82C620
Vendor	Intel	Philips	Thesys	TI	TI	MVL
CPU core	251	SIE	None	SIE	SIE	None
Ports	3 ports	4 ports	2 ports	4 ports	7 ports	4 ports
Internal port?	No	Yes	Yes	No	No	Yes
Package	PLCC-68	DIP-32	DIP-32	DIP-28	PQFP-48	PQFP-48
Availability	1Q97	Now	1Q97	Now	Now	Now
Price	$7	$6	$6	$4	$5	$5

Table 1. The current crop of USB hub- and peripheral controllers includes both intelligent and nonprogrammable parts from a variety of vendors. (Source: vendors)

Ports and Power Provide Differentiation

While support for four downstream ports seems to be the sweet spot, TI believes its seven-port hub will be in demand for home PCs that are used as entertainment systems. At least three ports are already used by the monitor, keyboard, and mouse. The extra ports could be used, for example, to connect multiple joysticks or multiple speakers to the same monitor or keyboard.

Power distribution is another factor separating hubs. In the USB lexicon, hubs are either self-powered (with their own power supply) or bus powered (drawing their current from the upstream device). Either way, the hub is responsible for providing power to all downstream USB connections. Those connections are classified as either high-power (up to 500 mA) or low-power (100 mA or less). Thus, each port on a hub must be able to source as much as 500 mA to each of its downstream devices. To avoid sapping too much current from the USB cable, bus-powered hubs cannot drive high-powered devices and are limited to only four low-powered devices; self-powered hubs can accept any number of high- or low-powered devices (see MPR 4/17/95, p. 1).

This maze of restrictions makes the monitor the attachment point of choice for PC hubs, because monitors generally have their own AC power supplies.

The Philips, TI, and Thesys chips work as either self-powered or bus-powered hubs. In their self-powered mode, they provide overcurrent protection on their downstream ports, as required by USB, with the help of external MOSFETs or other switching components.

The two TI chips go a bit further, managing port protection either individually or as a group. Group protection is easier to implement and requires fewer external components, but it has the disadvantage of lumping all downstream devices into a single load. If a single downstream device shorts, all downstream devices lose their power. Alternatively, each of the downstream ports can be handled individually, with separate power components for each.

Peripheral Controllers Also Proliferate

Outside of the host or hub market, a number of new peripheral controllers have appeared to handle leaf nodes. Many are keyboard-specific controllers, with a few generic USB converters thrown in.

Angling for keyboard design-ins is CMD's 0678KMp. The 48-pin device includes an 8051 with keyboard-controller firmware. In a unique twist, the 0678 accepts a standard PS/2 mouse connection, which will appear as a USB device to the upstream hub or host controller. The chip even supports hot-swapping the mouse.

Thesys's TH6503 is a simple device that acts as a USB-to-microcontroller bridge. The 16-pin chip carries USB signals on one side and a serial interface on the other. It's useful for adding USB to existing products or designs and could be used, for example, to add a USB interface to an existing keyboard or modem.

Price & Availability

Intel's 8x930Ax is currently in production at $6 in quantity. The 8x930Hx is sampling now for $7. For more information check *www.intel.com/design/usb.*

Philips's PDIUSBH11 hub controller is available for $6 in 10K quantities. The PDIUSBP11 in a 14-pin package costs $0.40. For more information contact Philips (Santa Clara, Calif.) at 800.447.1500, x1347.

Texas Instruments offers the 2040 and the 2070 for $4.10 and $5, respectively, in 1,000-unit quantities. Contact TI (Denver) at 800.477.8924, x5504.

Thesys will begin sampling the 6502 in March; pricing will be in the $4–$5 range. The 6503 is sampling, with pricing set at $1.65 in quantity. Contact Thesys (Erfurt, Germany) at 49.361.427.8100 or visit *www.thesys.de.*

CMD Technology's 0678KMp sells for $4.95. The 0670 is priced at $6.75. CMD Technology (Irvine, Calif.) can be reached at 714.454.0800, or visit *www.cmd.com.*

MultiVideo Labs is sampling its W82C620 controller. Contact MVL (Princeton, New Jersey) at 609.497.1930.

The Cypress CY7C63xxx family begins sampling in February with production in April. Contact Cypress (San Jose, Calif.) at 408.943.6300 or *www.cypress.com.*

Philips complements its hub chip with the PDIUSBP11, a peripheral controller like the TH6503 with a straightforward serial interface for controlling the peripheral device. The 'P11 comes in a 14-pin DIP and sells for about $0.40.

Cypress made its own 8-bit core for the CY7C63xxx controllers. While a standard SIE handles USB, the CPU adds local intelligence. Different version of the 63xxx family provide varying amounts of EPROM, SRAM, and I/O pins.

From Concept to Reality

Keyboards, mice, scanners, and speakers from Logitech, Cherry, KeyTronic, Altec Lansing, and others are now starting to appear on store shelves. With any motherboard based on a new chip set providing USB, the coming year will see this feature move from curiosity to common denominator.

Microsoft's operating systems have been slow to support USB, so silicon vendors have enjoyed a breathing period in which USB was neither in demand nor especially useful. That will change over the course of 1997 as public awareness of USB grows and PCs edge closer to appliance status.

By the end of 1997, USB will be a required feature on keyboards, high-end monitors, mice, and joysticks, at which time it will cease to be a differentiating factor. In the interim, USB provides an opportunity. Rather than just increasing the cost of mundane peripherals, USB can enable new devices, thus opening new markets. Digital speakers, inexpensive modems, and cheap networks are all new possibilities enabled by this new crop of USB microcontrollers. M

LITERATURE WATCH

BUSES

VME...then and now. VME started with Motorola's Jack Kister, who conceived the Versabus protocols for the 68000 CPU back in 1979 and 1980. Ray Alderman, VITA; *RTC,* 12/96, p. 40, 2 pp.

Laments of a dinosaur: reflections on the little bus that could...and did. Three significant factors made VME successful: its European birthplace; dedicated, talented, altruistic people; and a democratic, market-driven character. Pete Yeatman, The Yeatman Group; *RTC,* 12/96, p. 48, 5 pp.

VMEbus is business. Now, 15 years after VME was announced, business entities and structures that will address the requirements of OEMs and systems integrators for the end of the 20th century are falling into place. Warren Andrews, *RTC,* 12/96, p. 63, 2 pp.

VME extensions move the battle lines. Extensions to the VME64 specification, known as VME64x, provide features that would meet embedded real-time requirements well into the 21st century. John Rynearson, VITA; *RTC,* 12/96, p. 78, 4 pp.

VME sales top $1 billion: where to from here? VMEbus has shattered the record for merchant-market board sales and is expected to remain on a steady upward track, despite encroachment from competing technologies. Warren Andrews, *RTC,* 12/96, p. 91, 6 pp.

IC DESIGN

Chip patterning: it keeps going, and going, and... Optical lithography for IC processing was supposed to run out of steam somewhere around 1 micron. Fueled by new equipment and techniques, however, it's giving that battery bunny a run for its money. Jim Lipman, *EDN,* 12/19/96, p. 90, 3 pp.

Hybrid technology: a step ahead. Hybrid technology continues its time-honored tradition of edging out monolithic ICs. Bill Travis, *EDN,* 12/19/96, p. 96, 3 pp.

Low power, density, and better tools propel cell-based ASICs. Cell-based ASICs are fast becoming the number-one choice for system-level integration, with embedded arrays not far behind. Barbara Tuck, *Computer Design,* 12/96, p. 79, 7 pp.

Design services spreading with promise of speed and reduced risk. Design-services providers, now springing up around the industry, can satisfy your desire for faster time to market and reduced risk. Barbara Tuck, *Computer Design,* 12/96, p. 30, 3 pp.

Tool time for processor design. HP's workstation group uses automation in designing the PA-8000 microprocessor. Brian Arnold, Hewlett-Packard; *Integrated System Design,* 1/97, p. 18, 5 pp.

Focus report: floorplanners and physical design tools. New-breed floorplanners help bridge the gap between layout and synthesis. Steven E. Schultz, Texas Instruments; *Integrated System Design,* 1/97, p. 38, 5 pp.

MEMORY

SDRAMs poised for next performance leap. A directory of high-performance DRAMs. John H. Mayer, *Computer Design,* 12/96, p. 123, 4 pp.

MISCELLANEOUS

Windows challenges Unix engineering stronghold. Windows 95- and Windows NT-based workstations are moving in on turf once firmly held by Unix. Mike Donlin, Tom Williams, Rose Vines; *Computer Design,* 12/96, p. 59, 10 pp.

PROCESSORS

Microprocessor designers expand the envelope. At the recent Microprocessor Forum, the design community was wowed with several new-generation microprocessors. Bob Haavind, *Computer Design,* 12/96, p. 48, 1 pg.

PROGRAMMABLE LOGIC

Composing music on the PC: a new gig for reconfigurable computing. Two FPGAs form the heart of a low-cost digital audio system. The "proof of concept" for reconfigurable computing may put studio-level performance within the reach of garage bands. Fran Granville, *EDN,* 12/19/96, p. 37, 3 pp.

Performance, price cuts, ISP heat up the CPLD market. Fast, in-system programmable CPLDs are supported by standard design tools. Their price is nearly two times that of FPGAs. Dan Tanner, *Computer Design,* 12/96, p. 91, 5 pp.

FPGAs and drop-in modules. A design for a digital audio-transmission system is aided by existing core modules. Steven C. Durham, Brian J. Warren, CoDesign; *Integrated System Design,* 1/97, p. 30, 4 pp.

SYSTEM DESIGN

Cache strategies for microprocessor-based systems. Over the next few years, backside and inline architectures will become the new standards, while lookaside will be replaced by fast DRAM. Michael T. Peters, Sr., Motorola; *Computer Design,* 12/96, p. 38, 3 pp.

Multiprocessing issues in large systems. When building a large multiprocessor system, you have to account for memory architecture, communications efficiency, reliability, and ease of use. Richard Jaenicke, Sky Computers; *Computer Design,* 12/96, p. 51, 3 pp.

Chip technology fuels more realistic electronic games. Higher-performance microprocessors and 3D graphics engines are yielding results that approach computer-generated movie graphics. Bob Margolin, *Computer Design,* 12/96, p. 101, 4 pp.

Memory protection in embedded systems. A number of 32-bit processors available for embedded systems development are equipped with MMUs. Here's how to use memory management to survive software faults. Dan Hildebrand, QNX Software Systems; *Embedded Systems Programming,* 12/96, p. 72, 5 pp.

RECENT IC ANNOUNCEMENTS

PART NUMBER	VENDOR	DESCRIPTION	PRICE/QUANTITY	AVAILABILITY
MICROPROCESSOR				
TLCS-870	Toshiba 800.879.4963	Microcontroller family with 8-bit cores operates from 1.8-V supply; with 4K–8K ROM, 256 bytes RAM, and 1.3-mA operating current.	$2.70/10,000	Prod.—Now
PIC16C64x	Microchip 602.786.7668	Family of 8-bit microcontrollers provide analog features, including two precision voltage comparators, voltage reference, and brown-out protection.	$4.10/1,000	Prod.—Now
68HC11EA9 68HC11KW1	Motorola 512.328.2268	Two 8-bit microcontrollers are designed for automotive applications such as A/C, windows, central locking; with PLL and UART.	$6.79/10,000	Prod.—Now
INTERFACE				
PCI1250	TI 800.477.8924	PCI-to-CardBus controller handles transfers at 130M/s, approaching theoretical limit of PCI bandwidth; includes power management.	$16.52/100,000	Samples—Now Prod.—2Q97
Am79C989	AMD 408.749.5703	Physical-layer chip lowers cost of 10BASE-T Ethernet switches by integrating four ports with auto-negotiation for full-duplex capability.	$9.50/10,000	Samples—Now Prod.—2Q97
CXD1947Q	Sony 408.955.6572	Host controller for IEEE-1394 (FireWire) applications has PCI interface, transmits and receives isochronous or asynchronous data packets.	$50/1	Samples—1Q97 Prod.—2Q97
CXD1944R	Sony 408.955.6572	Physical-layer interface chip supports 200-Mbps IEEE-1394 transfers to/from host controller; handles arbitration and initialization functions.	$25/1	Samples—1Q97 Prod.—2Q97
PDI1394L11	Philips 800.447.1500	Link-layer controller for IEEE-1394 interfaces meets IEC 1883 specs for transporting digital video over IEEE-1394; with byte-wide interface.	$11/10,000	Prod.—Now
TC35821F	Toshiba 800.879.4963	ATM framer chip supports 155-Mbps transfers for routers and network-interface cards; with clock recovery, byte alignment, and frame sync.	$35/1,000	Samples—Now Prod.—1Q97
MEMORY				
HM5264405TT-10	Hitachi 800.285.1601	100-MHz synchronous DRAM has 64-Mbit capacity, organized as 8M×8 or 4M×16, with 3.3-V supply voltage; in TSOP-II package.	$90/1,000	Samples—1Q97 Prod.—2Q97
ISD33000	ISD 408.369.2400	Voice-recording memory adds auto-mute feature to eliminate recording of background noise; 1–1.5 or 2–4-minute capacity.	$7.95/50,000	Prod.—Now
X76F640	Xicor 408.432.8888	Flash memory has serial interface and data-security features, with 64-bit read and write passwords for separate blocks of data.	$3.95/10,000	Prod.—Now
25C080	Microchip 602.786.7668	Serial E^2PROM supports serial peripheral interface (SPI) with fast, 3-MHz data-transfer rate and 1.8–6.0-V operating supply; 8K capacity.	$1.08/1,000	Prod.—Now
MISCELLANEOUS				
HCS410	Microchip 602.786.7668	Code-hopping transponder and encoder for remote keyless entry systems combines security and small package; with 2.0–6.0-V supply range.	$1.36/10,000	Samples—1Q97 Prod.—2Q97
HCS500	Microchip 602.786.7668	Code-hopping decoder for remote keyless entry or access-control systems handles reception and validation of codes, learning new transmitters.	$1.17/5,000	Prod.—Now
STi4600	SGS-Thomson 617.259.0300	Dolby AC-3 decoder chip is capable of decoding 5.1-channel digital audio, satisfying all functional and performance parameters of AC-3 Class A.	$13.50/100,000	Prod.—Now
SYSTEM LOGIC				
SD6430	Sigma Designs 510.770.0100	Integrated RealMagic 3D video accelerator is designed to meet Direct3D and DirectDraw requirements; includes 24-bit RAMDAC.	$25/10,000	Prod.—Now
VxP195	AuraVision 510.252.6800	Chip simplifies integration of several non-PCI audio/video sources in a single PCI slot; with five DMA channels, I^2S interface, endian control.	$20/10,000	Samples—Now Prod.—2Q97

PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,553,276

Self-timed processor with dynamic clock generator having plurality of tracking elements for outputting sequencing signals to functional units
Issued: September 3, 1996
Inventor: Mark E. Dean
Assignee: IBM
Filed: August 31, 1994
Claims: 20
A method and system are provided for self-timed, asynchronous processing. An operation is executed with a function unit. A timing of the operation execution is simulated with a tracking element, and a tracking signal is output. A sequencing signal is varied to the function unit in response to the tracking signal.

5,553,256

Apparatus for pipeline streamlining where resources are immediate or certainly retired
Issued: September 3, 1996
Inventors: Michael A. Fetterman, et al
Assignee: Intel
Filed: June 5, 1995
Claims: 5
Maximum throughput or back-to-back scheduling of dependent instructions in a pipelined processor is achieved by maximizing the efficiency with which the processor determines the availability of the source operands of a dependent instruction through multiple, described mechanisms.

5,553,255

Data processor with programmable levels of speculative instruction fetching and method of operation
Issued: September 3, 1996
Inventors: Danny K. Jain, et al
Assignee: Motorola/IBM
Filed: April 27, 1995
Claims: 6
A data processor with branch-prediction unit that predicts conditional branch instructions and a control unit that monitors the number of unresolved branch instructions. The control unit is allowed to fetch instructions indicated by the branch-prediction unit, depending upon the number of unresolved branch instructions. The number of unresolved branch instructions is user programmable.

5,548,737

Dynamic load balancing for a multiprocessor pipeline by sorting instructions based on predetermined execution time
Issued: August 20, 1996
Inventor: Jimmie D. Edrington, et al
Assignee: IBM
Filed: April 11, 1995
Claims: 28
An apparatus for processing high-level instructions, including multiple processing units, means for generating a plurality of instructions to perform the high-level instructions, and means for dynamically organizing the generated instructions into at least one group, each group including at least one instruction to be processed by one of the processing units. In addition, a method of processing high-level instructions by multiple processing units, including generating multiple instructions to perform the high-level instructions and dynamically organizing those instructions into groups.

5,546,552

Method for translating non-native instructions to native instructions and combining them into a final bucket for processing on a host processor
Issued: August 13, 1996
Inventors: Brett Coon, et al
Assignee: Seiko Epson
Filed: May 12, 1995
Claims: 7
System and method for extracting complex, variable-length computer instructions, each subdivided into a variable number of instruction bytes, and aligning instruction bytes of instructions. The isolated complex instructions are decoded into nano-instructions that are processed by a RISC processor core.

5,546,545

Rotating priority-selection logic circuit
Issued: August 13, 1996
Inventor: Stephen E. Rich
Assignee: IBM
Filed: December 9, 1994
Claims: 6
A rotating priority-selection circuit selects the oldest instruction with ready operands for execution in a microprocessor that allows for out-of-order execution.

OTHER ISSUED PATENTS

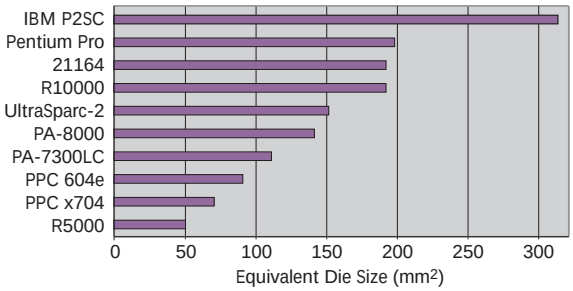
5,548,736 *Method and apparatus overcoming delay introduced by instruction interlocking in pipelined instruction execution*
5,546,599 *Processing system and method of operation for processing dispatched instructions with detected exceptions* M

CHART WATCH: WORKSTATION PROCESSORS

	Digital 21164	IBM P2SC	Exponential PPC x704	PowerPC 604e	Sun Ultra-2	HP PA-8000	HP PA-7300LC	MIPS R10000	MIPS R5000	Pentium Pro
Clock rate	500 MHz	135 MHz	**533 MHz**	225 MHz	250 MHz	180 MHz	160 MHz	200 MHz	180 MHz	200 MHz
Cache size	8K/8K/96K	**32K/128K**	2K/2K/32K	32K/32K	16K/16K	None	64K/64K	32K/32K	32K/32K	8K/8K
Issue rate	4 issue	**6 issue**	3 issue	4 issue	4 issue	4 issue	2 issue	4 issue	1+FP	3 x86 instr
Pipe stages	7 stages	5 stages	6 stages	6 stages	6/9 stages	7–9 stages	5 stages	5–7 stages	5 stages	**12–14**
Out of order	6 loads	5 instr	None	16 instr	None	**56 instr**	None	32 instr	None	40 ROPs
Rename regs	None	22 fp	None	12 int/8 fp	None	56 total	None	**32/32**	None	40 total
BHT entries	**2K × 2-bit**	None	256 × 2-bit	512 × 2-bit	512 × 2-bit	256 × 2-bit	None	512 × 2-bit	None	≥512
TLB entries	48 I/64 D	64 I/64 D	128 unified	**128/128**	64 I/64 D	96 unified	96 unified	64 unified	48 unified	32 I/64 D
Memory b/w	~400 MB/s	**2.2 GB/s**	~270 MB/s	~180 MB/s	1.3 GB/s	768 MB/s	213 MB/s	539 MB/s	~160 MB/s	528 MB/s
Package	CPGA-499	**SCC-1,088**	CBGA-359	CBGA-255	CPGA-521	LGA-1,085	CPGA-464	CPGA-527	SBGA-272	MCM-387
IC process	0.35µ 4M	**0.27µ 5M**	0.5µ 5M§	0.35µ 4M	0.29µ 4M	0.5µ 4M	0.5µ 4M	0.35µ 4M	0.35µ 3M	0.35µ 4M
Die size	209 mm²	335 mm²	150 mm²	148 mm²	149 mm²	**345 mm²**	259 mm²	298 mm²	84 mm²	196 mm²
Transistors	9.3 million	**15 million**	2.7 million	5.1 million	3.8 million	3.9 million	9.2 million	5.9 million	3.6 million	5.5 million
Est mfg cost*	$150	**$375**	$90	$60	$90	$290	$95	$160	$25	$175‡
Power (max)	25 W	30 W	**85 W**	20 W*	20 W	>40 W	15 W	30 W	10 W	35 W‡
SPEC95b†	**12.6/18.3**	5.9/15.4	12/10	9.0/8.5*	8.5/15	10.8/**18.3**	7.3/7.4	10.7/17.4	4.7/4.7	8.7/6.0‡
Availability	4Q96	3Q96	2Q97	3Q96	Limited	2Q96	3Q96	1Q96	1Q96	2Q96‡
1K list price	$1,450	Not public	$1,000*	$594	$1,995	Not public	Not public	**$3,000**	$365	$1,217‡

†SPEC95 baseline (int/FP) ‡includes 512K L2 cache §bipolar + CMOS (Source: vendors except *MDR estimates)

The table above gives the vital statistics for the key RISC processors available today or by midyear. The table below provides performance data on the full SPEC95 benchmark suite for currently shipping processors that have reported SPEC95 results. The graph attempts to compare processor die sizes as if all the chips were built in Intel's P854 (0.35-micron four-layer-metal) process.



Processor	Digital 21164	HP PA-8000	MIPS R10000	Intel PPro	PowerPC 604e	HP 7300LC	Sun UltraSparc	Intel P55C	IBM P2SC	MIPS R5000
System	AlphaSta. 500/500	HP9000 K460EG	Siemens RM400 C90	ICL J650i	Motorola 2604	HP Visual. Mod B160L	Sun Ultra 2/1200	Dell XPS	IBM 595 RS/6000	Siemens RM300 C40
Clock rate	500 MHz	180 MHz	200 MHz	200 MHz	200 MHz	160 MHz	200 MHz	200 MHz	135 MHz	180 MHz
Ext. cache	2M	2M	4M	512K	256K	1M	1M	512K	none	512K
099.go	16.0	11.8	11.1	8.54	9.89	9.80	8.24	7.19	8.00	4.99
124.m88Ksim	12.6	11.6	9.81	7.80	7.12	6.82	5.89	7.24	4.67	4.61
126.gcc	10.7	9.33	10.7	8.22	7.63	7.16	7.76	6.47	6.20	4.78
129.compress	11.2	10.6	11.1	8.21	7.80	6.24	8.44	4.55	5.55	4.63
130.li	10.7	11.4	10.7	9.29	7.16	7.43	5.89	7.18	5.21	4.52
132.ijpeg	13.9	9.97	9.97	8.42	9.81	5.81	6.95	4.16	7.44	4.31
134.perl	14.3	10.4	11.7	9.11	9.01	8.08	5.92	9.17	5.33	6.21
147.vortex	12.1	11.5	10.9	10.3	7.71	7.91	6.71	6.79	5.40	3.89
SPECint95b*	**12.6**	**10.8**	**10.7**	**8.71**	**8.20**	**7.32**	**6.90**	**6.41**	**5.88**	**4.70**
101.tomcatv	24.2	30.4	24.5†	8.91	10.1	11.1	20.1	6.96	33.3	6.16‡
102.swim	25.5	30.2	32.2†	12.4	15.3	17.9	27.6	7.71	39.8	8.94‡
103.su2cor	10.3	12.8	10.5†	3.89	4.39	3.66	7.88	2.79	6.44	1.92‡
104.hydro2d	13.7	10.6	10.4†	3.69	4.51	3.86	6.44	2.66	8.34	2.08‡
107.mgrid	17.7	15.4	18.5†	3.30	6.20	5.64	10.1	1.87	12.9	4.11‡
110.applu	8.30	15.2	12.2†	3.28	6.23	4.99	7.02	1.99	12.9	3.60‡
125.turb3d	20.3	12.9	12.1†	5.78	9.99	6.70	7.26	4.15	13.7	4.66‡
141.apsi	18.7	12.3	15.9†	6.75	7.74	7.69	10.3	4.26	8.73	4.65‡
145.fpppp	37.4	32.1	26.8†	10.7	18.7	12.4	14.8	5.47	20.2	14.9‡
146.wave5	22.7	28.3	25.3†	7.74	7.05	9.54	12.5	5.69	25.7	5.22‡
SPECfp95b*	**18.3**	**18.3**	**17.4†**	**5.95**	**8.09**	**7.38**	**11.1**	**3.90**	**15.4**	**4.72‡**

*SPEC95 baseline results †measured on SGI Origin 2000 ‡measured on SGI Indy R5000 (Source: vendors, SPEC)

RESOURCES

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Whether it's for a round of golf or a glimpse into the future of mobile computing platforms, Mobile Insights '97 has what senior executives are looking for. The annual conclave, held at the Ritz-Carlton in Laguna Niguel (Calif.) and running February 23–25, serves up three days of hands-on product demonstrations and presentations as well as the evening's Mobility Awards. Attendees get free use of an NEC MobilePro HPC during the course of the show.

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