Intel Prepares MMX CPU Wave

After Weak 1996, AMD and Cyrix Ready 1997 Counterstrike

A Look Back
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A Look Ahead

by Michael Slater

The past year has been a remarkably successful one for Intel and a difficult one for its competitors. It was a quiet year for Intel in terms of new products, but the company nevertheless increased both its market share and its gross margin—thanks, in large part, to weak performances from AMD and Cyrix. (See sidebar on page 8 for a summary of the key events of 1996 and pointers to MPR's coverage.)

Next year promises to be far more turbulent. Not only will Intel introduce two major new product lines—P55C and Klamath—but AMD and Cyrix will each launch their own next-generation processors, which will be more formidable competitors to Intel's line. Intel is sure to do well despite the stepped-up challenge, but its dominance of the market is unlikely to be quite as complete in 1997 as in 1996.

Intel Shifting into High Gear

In the past year, Intel's microprocessor lineup changed little. After the introduction of the 150- and 166-MHz Pentiums in January, the only new products were the 200-MHz Pentium and 150-MHz Mobile Pentium. The P55C would have been a great kicker for fall sales, but Intel apparently didn't have the part ready in time. Intel began producing P55C processors in the late fall but chose not to announce the part until January in order to minimize the impact on the Christmas selling season. It was too early in the P55C's life cycle to service the Christmas demand, and some system makers wanted a chance to sell their Pentium inventory.

Although Pentium Pro got lots of publicity, it played a minor role in the market: Intel shipped fewer than 3 million Pentium Pros during 1996, compared with more than 60 million Pentiums.

There were no announcements at all in the Pentium Pro line during 1996, in part because Intel pre-announced six months worth of products to make a big splash at Pentium Pro's late 1995 introduction.

Pushing the processor beyond 200 MHz apparently wasn't possible; although the CPU chip could probably reach 233 MHz, speed limits on the L2 cache chip kept Intel from introducing a faster Pentium Pro.

Following the 1996 lull, the first half of 1997 will see a rush of new products from Intel. The P55C will be officially launched on January 8, marking the debut of MMX and Intel's shift away from the BiCMOS process it has used since the first Pentium. This processor will be followed in the second quarter by Klamath—the product that will bring the P6 into the high-volume market and introduce PC board modules as Intel's standard processor packaging.

Figure 1 shows Intel's past price trends and our projections for the coming year. Intel cut prices with its traditional aggressiveness in the first half of the year, but in the second half of the year Intel's pricing was essentially flat. Intel attributed the absence of the 4Q96 price cut to a desire to maintain stability for PC makers during the Christmas season. Although this was no doubt one consideration, the fact that
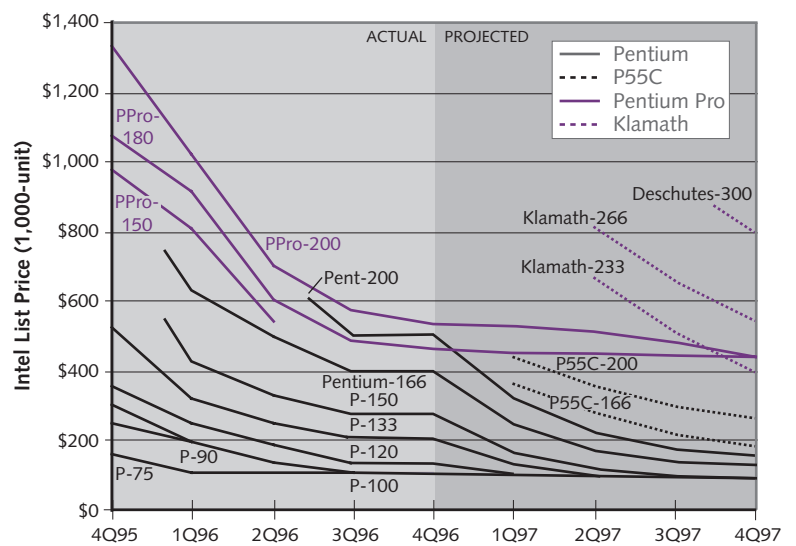

Figure 1. Intel's prices stabilized in 2H96 but will begin dropping again as the next-generation chips roll out. (Source: Intel, MDR projections)

x86 Processors

Intel was selling everything it could make and had no strong competition surely played a part in the decision.

The P55C will take over the high-end Pentium price points, pushing the Pentium-166 and -200 down to entry-level prices. The 100-MHz Pentium will all but disappear by mid-year, while the 133-MHz part takes the economy spot and the 166-MHz version becomes the mainstream entry-level chip. The 120- and 150-MHz Pentiums, with their slower 60-MHz bus, will fade away quickly. Intel could push the P55C to higher clock rates, but it is likely to limit this part's speed, at least on the desktop, to encourage migration to the P6 family.

In response to weak demand early in the year, Intel aggressively cut Pentium Pro prices last spring. This succeeded in spurring demand, but Intel kept most of its wafers allocated to the more profitable Pentium. As a result, Intel has been capacity constrained on Pentium Pro for the past few months. We expect Pentium Pro prices to remain relatively stable, shifting demand to Klamath.

Klamath initially will boost P6-family pricing to levels Intel enjoyed in 1H96, but the company is likely to bring Klamath prices down rapidly as it moves this part into the main-stream. By early 1998, Deschutes—a 0.25-micron shrink of Klamath with clock rates of 300 MHz and higher—will take over the high-end performance and price points.

Table 1 summarizes key characteristics of the processors that will fuel the PC market in 1997. Of the new processors, all except AMD's K6 are based on existing cores, and all except Cyrix's GX86 include the MMX extensions.

Pentium Pro to Survive Klamath Rollout

At first glance, it seems Klamath should obsolete Pentium Pro. Intel expects, however, that PPro will continue to hold a place in the market, at least through the end of 1997, with more shipments in 1997 than in 1996. This will be driven, in part, by inertia; since Klamath requires new motherboard designs—and in some cases, even new chassis designs to accommodate the daughtercard—existing PPro systems won't be easily converted to Klamath and will continue to sell for some time. A 200-MHz PPro may also outperform a 233-MHz Klamath on applications that benefit from the faster L2 cache and don't use MMX.

It seems likely that Intel will position Klamath as a desktop and low-end server part initially, with Pentium Pro focused on midrange and high-end servers. Sources indicate that Intel is not supporting Klamath for systems with more than two processors, so four-way multiprocessor systems will

	Intel				AMD		Cyrix		
	Pentium (P54C)	Pentium/MMX (P55C)	Pentium Pro	Klamath	K5	K6	6x86 (M1)	M2	GX86
Interface	Pentium	Pentium	P6	P6 + L2 cache bus	Pentium	Pentium	Pentium	Pentium	custom
MMX?	no	yes	no	yes	no	yes	no	yes	no
L1 Cache (I/D)	8K/8K	16K/16K	8K/8K	16K/16K	16K/8K	32K/32K	16K unified	64K unified	16K unified
L2 Cache	none	none	256K or 512K in package	256K or 512K on module	none	none	none	none	none
L2 Cache Bus	none	none	at CPU speed	1/2 CPU speed	none	none	none	none	none
Basic Pipeline	5 stages	6 stages	12 stages	N.D.	6 stages	6 stages	7 stages	7 stages	6 stages
Out of Order?	no	no	yes	yes	yes	yes	limited	limited	no
Peak Decode Rate	2 instr	2 instr	3 (2 simple+ 1 complex)	N.D.	4 instr (1 in prefetch)	2 instr	2 instr	2 instr	1 instr
BTB	256 entry	256 entry	512 entry	N.D.	1,024 BHT	8,192 BHT	256 entry	512 entry	128 entry
TLB (I/D)	32/64 entry	32/64 entry	32/64 entry	N.D.	128 entry	128/64 entry	128 entry L1 8 entry L2	16 entry L1 384 entry L2	32 entry
Return Stack	none	4 entry	4 entry	N.D.	none	16 entry	8 entry	8 entry	8 entry
Write Buffer	2 entry	4 entry	N.D.	N.D.	4 entry	N.D.	8 entry	8 entry	8 entry
Core Voltage	3.3 V 2.9 V mobile	2.8 V 2.5 V mobile	3.3 V	2.8 V	3.5 V	2.9 V	3.3 V	2.5 V	3.3 V
Typical Power	3.9–6.5 W	5.5–7.3 W	23.0–32.6 W	N.D.	7.9–10.6 W	N.D.	14.8–21.1 W	N.D.	N.D.
Max Power	10.1–15.5 W	9.5–15.7 W	29.2–37.9 W	N.D.	10.3–13.7 W	N.D.	17.8–24.6 W	N.D.	N.D.
IC Process	0.35µ 4M BiCMOS	0.28µ 4M CMOS	0.35µ 4M BiCMOS	0.28µ 4M CMOS	0.35µ 3M CMOS	0.35µ 5M CMOS	0.44µ 5M CMOS	0.35µ 5M CMOS	0.35µ 3M CMOS
Transistors	3.3 million	4.5 million	5.5 million	7.5 million	4.3 million	8.8 million	3.0 million	6.0 million	1.9 million
Die Size	90 mm²	140 mm²	196 mm²	203 mm²	177 mm²	162 mm²	169 mm²	197 mm²	144 mm²
Est Mfg Cost*	$40	$50	$145†	$80	$70	$80	$70	$90	$60
Clock Speeds	100–200 MHz	166–200 MHz	150–200 MHz	233–266 MHz*	75–100 MHz	180–233 MHz	100–150 MHz	180–225 MHz	120–166 MHz
Perf/MHz*	1	1.1	1.4	1.35	1.25	1.45	1.2	1.3	0.9
Availability	now	Jan 97	now	2Q97*	now	1Q97	now	2Q97	1Q97
Price (1,000)	$106–$509	N.D.	$534–$1,035	N.D.	$65–$101	N.D.	$98–$299	N.D.	N.D.

Table 1. Key specifications for 1997's crop of x86 processors. The Perf/MHz metric is MDR's estimate of average performance for 32-bit applications that do not use MMX. Power and price ranges correspond to clock-speed range shown; lower P55C power is for mobile version; higher PPro power is with 512K L2. N.D. = not disclosed; †includes 256K cache. (Source: vendors, except *MDR estimates)

remain a PPro stronghold until Deschutes ships. In server applications, Klamath's half-speed L2 cache is a bigger hindrance than on the desktop, strengthening PPro's position in servers. A version of PPro with a 1M L2 cache is rumored to be in the works and would further establish PPro as the preferred server solution. By 1998, however, Deschutes modules running at 300 MHz with L2 caches of 1–2M are likely to displace Pentium Pro in servers.

Intel Lineup Leaves Notebook Hole

As diverse as Intel's product line will be in 1997, it leaves one significant hole: a P6-class processor for notebooks. As Figure 2 shows, the P55C will be Intel's fastest mobile offering in 1997; Klamath's power consumption will be too high for reasonable notebooks. Although the P55C-166 offers a modest boost from the existing mobile Pentiums, it leaves a significant gap between high-end notebook and desktop performance. Deschutes will run at a lower supply voltage and enable a mobile P6 processor. Deschutes won't be in production until late 1997, however, and it won't be until sometime in 1998 that a mobile Deschutes processor will be available.

Processors that provide P6-class performance in a P55C socket and with P55C power consumption could present a major opportunity for AMD and Cyrix—if they can deliver them before notebook makers make the switch to Deschutes. Notebook PC makers are unhappy with being left more than two years behind the desktop in getting to the P6 generation, and they are looking for something to keep their products moving up in performance after the P55C. AMD's K6 and Cyrix's M2 both have a shot at this opportunity.

The long delay before the introduction of mobile P6 processors may prompt Intel to push the P55C speed further. By shrinking the P55C to the 0.25-micron process, which we expect Intel to have ready for production in the second half of the year, the supply voltage could be lowered further. This change would enable a 200-MHz P55C derivative to fit within the mobile power envelope.

Extending the Life of the P55C Pinout

Cyrix and AMD have both stayed with the P55C pinout (also called the Socket 7 interface). For a uniprocessor system, the Pentium bus is just as good as—if not better than—the P6 bus. It also has far more chip sets available, and they are less expensive. Whereas Klamath will require entirely new motherboards, the K6 and M2 will plug into existing Pentium or P55C designs with little or no modification. AMD and Cyrix do not expect any role in multiprocessor systems.

What the Pentium interface lacks, however, is a separate bus for the L2 cache. While Pentium Pro runs its L2 cache interface at up to 200 MHz and Klamath runs it at 117–133 MHz (for 233–266 MHz processors), all devices that fit into the Pentium socket are limited to a single, slower bus shared by main memory and the L2 cache.
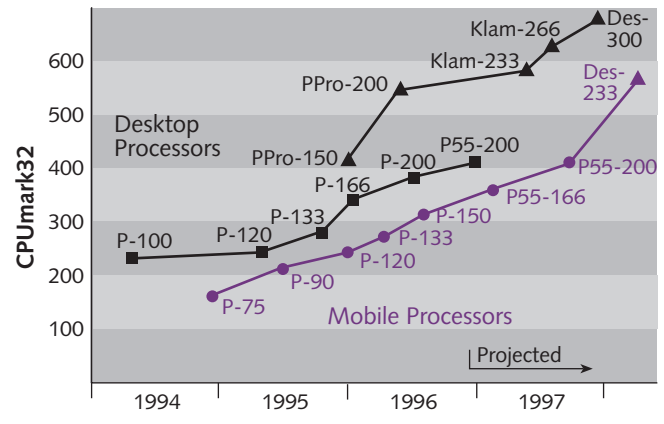
To reduce the effect of the slower L2 interface, both the

Figure 2. Peak mobile processor performance (in purple) has lagged desktop levels by 6–9 months, but the P6 line is widening the gap (Klam = Klamath; Des = Deschutes). (Source: Intel for current processors; MDR estimates for P55C, Klamath, Deschutes)

K6 and the M2 have a total of 64K of on-chip, level-one cache—twice that of the P55C or Klamath. The chips also have larger TLBs and return stacks. As core CPU speeds increase, the relatively slow L2 interface will become more of a limitation for Pentium-pinout chips.

To address this weakness without moving to a new pinout, Cyrix supports a 75-MHz bus for the 150-MHz 6x86 and 225-MHz M2. AMD is also investigating faster bus speeds. One problem with the 75-MHz bus is that it requires the PCI bus to either run asynchronously, losing cycles to synchronization delays, or at 25 MHz. The best solution, albeit hard to implement, would be a 100-MHz CPU bus. This would provide a significant bandwidth boost while allowing the PCI bus to run at one-third of the CPU bus rate.

AMD and Cyrix must contend not only with the rapid pace of Intel's new product introductions but also with the evolution of the platform. In 3Q97, the first systems with the Advanced Graphics Port (AGP) are expected, and Intel is sure to heavily promote this feature as a "must have" for users interested in 3D graphics. Its actual benefit remains to be seen, and PCI-based graphics cards will serve the market quite well for some time, but Intel is nevertheless likely to invest heavily in creating demand for AGP—which Intel will support only on Klamath, not on Pentium-family systems.

AMD and Cyrix are well aware of the need for system-logic chips that offer AGP with Pentium-bus systems. Cyrix is counting on AGP chip sets from SiS and VIA that will support the Pentium bus and AGP. AMD is rumored to be creating its own chip-set designs to ensure that lack of AGP chip sets won't hinder the success of the K6. The company also has an active program, called FusionPC, to support outside chip-set vendors. AMD might even offer some of its Fab 25 capacity to selected vendors. Access to advanced process technology could be a significant factor in enabling chip-set vendors to support higher CPU bus speeds.

Key x86 Events of 1996

Intel introduced 150- and 166-MHz Pentium chips (1001MSB.PDF).

Intel was embarrassed to find that a bug in its compiler had erroneously inflated Pentium's SPECint92 ratings by about 10% (1001MSB.PDF).

Intel and AMD reached a patent agreement that includes rights to MMX but limits use of the P6 bus (1001MSB.PDF).

UMC of Taiwan agreed to withdraw from the 486 market to settle its litigation with Intel (1001MSB.PDF).

Cyrix and IBM raised 6x86 clock speeds to 133 MHz for P-166 performance (1002MSB.PDF).

Intel disclosed the MMX instruction set extensions more than nine months before the debut of the P55C (1003MSB.PDF).

Intel announced a 133-MHz mobile Pentium and introduced Pentium OverDrive processors for 75- and 90-MHz systems (1003MSB.PDF).

AMD shipped its delayed K5 first at 75 and 90 MHz (1004MSB.PDF).

A few months after purchasing NexGen, AMD officially dropped the Nx586 (1004MSB.PDF).

Cyrix went into the mail-order PC business to build its brand image (1004MSB.PDF, and 1005MSB.PDF).

AMD boosted the K5 to 100 MHz (1006MSB.PDF).

Cyrix and IBM launched a 150-MHz, P200 version of the 6x86 (100801.PDF).

Intel boosted Pentium to 200 MHz (100801.PDF).

Intel updated its iCOMP performance metric to version 2.0 (100902.PDF).

Intel added a 150-MHz mobile Pentium and cancelled its 4Q price cut (1010MSB.PDF).

A bug in the 6x86 cache caused a performance problem when running Windows NT 4.0 on early versions of the chip (1011MSB.PDF).

International Meta Systems said it will have a Pentium competitor by the end of 1997 (1012MSB.PDF).

AMD's enhanced K5 debuted with Pentium-133 performance at 100 MHz (1013MSB.PDF).

Intel disclosed the P55C microarchitecture at the Microprocessor Forum (101404.PDF).

AMD described its K6 at the Microprocessor Forum (101406.PDF).

Cyrix disclosed its M2 at the Microprocessor Forum (101405.PDF).

Rumors surfaced of Intel's Katmai and Willamette P6-family follow-ons (1015MSB.PDF).

AMD previewed a K5-PR166 and a 200-MHz K6 at Comdex (1016MSB.PDF).

Intel revealed its plans for Klamath daughtercards (1016MSB.PDF).

Cyrix to Drop Back from High-End Attack

Cyrix's 6x86 was rolled out with great fanfare early this year, touted as the first compatible processor to outperform Intel's Pentium line. Cyrix's 133-MHz part outperforms the Pentium-166 by a few percent on Winstone 96, and the 150-MHz version—with a 75-MHz bus—provides a similar edge over the Pentium-200.

Despite its impressive performance, the 6x86 took off quite slowly. Samples were shipped in late 1995, but revisions to the chip delayed full production until 1Q96. Cyrix and its partner IBM Microelectronics found it much harder than they expected to sell the chip to top-tier PC makers, who didn't find the 6x86 appealing enough to stray from the Intel fold. Not until the third quarter did sales begin to pick up, thanks to aggressive pricing and a shift in the sales strategy toward second- and third-tier PC makers. Cyrix's only other product was the 5x86, which sold at low prices and was phased out in the second quarter, so the delay in ramping up the 6x86 left Cyrix with some very lean quarters. The company's troubles led to the resignation of its president and founder, Jerry Rogers, earlier this month.

IBM continues to be Cyrix's primary foundry. Cyrix's second foundry, SGS-Thomson, originally promised to begin 6x86 production in 2Q96 but is still struggling to achieve acceptable yields. Cyrix has also been building test chips at more than one Asian foundry, although no production relationship has been disclosed.

Cyrix continues to refine the 6x86 design in advance of the next-generation M2. The 6x86L, built in IBM's 0.33-micron CMOS-5X, will cut the supply voltage from 3.3 V to 2.8 V for desktop systems, bringing the power dissipation more in line with Intel's and AMD's chips. Seeking to expand the 6x86 market to notebook computers, Cyrix has sampled a 2.35-V version, called the 6x86LV. Cyrix will offer a BGA package as an alternative to Intel's TAB package.

Thanks to very aggressive pricing, 6x86 volume took off in the fourth quarter. Cyrix will have to keep cutting prices to maintain its position in the first half of next year, as Intel is likely to slash P54C prices to make room for the P55C. Cyrix will continue to position the 6x86 against the P54C, while the M2 will hold a similar position against the P55C.

Cyrix's M2 enhances the 6x86 CPU with four times as much on-chip cache, larger TLBs, MMX, and a faster FPU. Cyrix and IBM expect to sample the M2 in the first quarter, with limited production in the second quarter and volume production ramping up in the third quarter.

The M2, if it meets its performance goals, should be a strong competitor for the P55C. Cyrix expects to deliver greater performance at the same clock speed, as well as offering higher clock speeds. Whether it is up to competing against Klamath is another question; it appears Klamath will have a significant lead in clock speed and will offer dramatically faster floating-point, which is increasingly important in consumer PCs because of the emergence of 3D games that perform real-time rendering.

Driving Down Cost with the GX86

In addition to boosting performance with the M2, Cyrix is chasing cost-sensitive markets with the GX86. This part, first disclosed at the 1995 Microprocessor Forum (see 091403.PDF), was originally expected to go into production in the first half of 1996 but has been delayed until early 1997. It combines a 5x86 core with a unified-memory graphics controller, a PCI bus interface, and a 64-bit-wide DRAM controller. The high integration trims system cost by eliminating the graphics controller, the "north bridge" system-logic chip (which interfaces the processor to DRAM and PCI), and the graphics memory.

The 5x86 core in the GX86 is slower than Pentium, but Cyrix expects the on-chip graphics and DRAM controller will enable the part to perform comparably on a per-clock basis to a typical Pentium system (without L2 cache). Initial offerings will be at 120 and 133 MHz, with future products planned all the way up to 200 MHz.

If Cyrix can find OEM partners to pursue this strategy, the GX could become a significant force in the entry-level computer market. (Compaq is rumored to have a system design based on the GX86 under way.) It could also play a role in the emerging NetPC market. The GX86 would have been a stronger product in mid-'96 than it will be in mid-'97, however; as Intel's product line has moved forward, the relative performance of the GX has slipped. At the same time, graphics chips have become cheaper and more capable, the cost of graphics memory has plummeted, and MMX has entered the fray.

The good news and the bad news about the GX86 is that it is unique. Because it requires a custom motherboard design, design wins will be harder to come by than for the 6x86 and M2. On the other hand, Intel has no directly competitive device; the GX86 could be the lowest-cost solution for entry-level systems. Cyrix also won't have to compete with its partner IBM, which has no plans to sell the GX86 under its own name.

K6 to Be AMD's Salvation

AMD's 486 (aka the 5x86) and K5 kept the company in the x86 business in 1996, but with paper-thin margins and a narrow, low-end product line. AMD kept to the plan it laid out after the major slip in the program in mid-1995, shipping 75- and 90-MHz parts in 2Q96 and 100-MHz chips in 3Q96. These chips offer performance that is essentially the same as the Intel chips of the same clock speed.

The most significant K5 development was AMD's shipment of a revised design in the third quarter that offered Pentium-133 performance while running at 100 MHz. The enhanced K5 has proved faster than the 6x86 on a per-clock basis, although AMD's clock speeds remain more limited. AMD is now sampling a 116.7-MHz version (using a 1.75 bus multiplier) that delivers Pentium-166 performance; it will be in production in 1Q97. A 133-MHz, P-200 version is likely to follow.

	Intel P55C	Klamath	Cyrix M2	AMD K6
Max. Issue	2 instr.	N.D.	1 instr.	1 instr.
ALUs	2 units	N.D.	1 unit	1 unit
Shifters	1 unit	N.D.	1 unit	1 unit
Multipliers	1 unit	N.D.	1 unit	1 unit
Multiply Thruput	1 cycle	1 cycle	1 cycle	1 cycle
Multiply Latency	3 cycles	3 cycles	2 cycle	1 cycle
Mul-add Thruput	1 cycle	1 cycle	1 cycle	1 cycle
Mul-add Latency	3 cycles	3 cycles	2 cycle	2 cycles

Table 2. Intel's processors can issue two MMX instructions in the same cycle, but Cyrix and AMD both have smaller latencies for multiply and multiply-add. (Source: vendors)

The key to AMD's future is the K6, which the company has already sampled and expects to begin shipping in 1Q97. A derivative of NexGen's 686, which was never produced in its original form, the K6 is the most aggressive CPU design to fit into a P55C socket. AMD once planned to create the K6 by enhancing the K5 design, much as Cyrix's M2 is an enhanced 6x86. Delays with the K5, as well as disappointing performance from the initial design, led AMD to acquire NexGen to get a more advanced design to serve as the basis for the K6.

Although benchmark results have not been disclosed, demonstrations have shown the K6 running Windows NT to exceed Pentium Pro's performance (with both processors running at 200 MHz), at least on the applications AMD chose to show. AMD expects to have parts at 180, 200, and 233 MHz at introduction. If achieved, these speeds would put the K6 in the same performance range as Klamath. If Klamath is initially offered at 266 MHz, that part would probably have an edge over AMD, but the K6 will be moved to AMD's 0.25-micron CS44 process by 4Q97. In that process, speeds of 300 MHz and up are possible—just in time to compete with Deschutes.

AMD will continue to promote the K5 for entry-level systems. The company is likely to start by pricing the K6 against P55C and Klamath, but there is plenty of room to bring the K6 down to volume prices as circumstances warrant. AMD has devoted Fab 25 to the x86 line; it will be ramping up to 6,300 wafers per week by the 2H97, providing enough capacity to produce tens of millions of processors per year.

MMX a Nearly Universal Feature

All the processors with MMX implement the same instruction set, at least in theory. Intel published the MMX instruction-set definition in March, enabling AMD and Cyrix to design MMX-compatible processors for introduction soon after Intel's own P55C. Intel could easily have waited until the chip's announcement to publicly disclose the details, but the company decided that encouraging widespread adoption of MMX was more important than using it as a competitive edge against AMD and Cyrix. The fact that Microsoft has been reluctant to use any Intel-specific features may have helped sway Intel to its relatively open position.

As Table 2 shows, there are performance differences among the various MMX implementations. Intel's are the
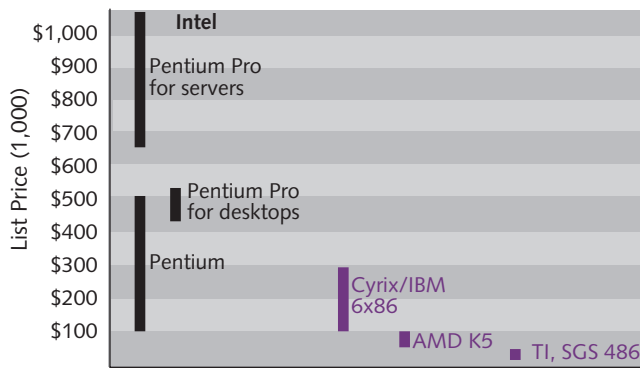
Figure 3. Intel's processors span a wide price range, with an average selling price of $200–$250, while its competitors are struggling at much lower price points. (Source: vendors)

only processors with dual MMX pipelines, allowing ALU operations to be issued at a rate of two per cycle. Intel's P55C multiplier has the longest latency of the group, however. The P55C is also the slowest of the designs in the time required to switch between floating-point and MMX contexts. The significance of these differences remains impossible to evaluate until MMX applications are available.

Cyrix, AMD Struggle with Price Points

As Figure 3 shows, Intel's competitors have been confined to a much narrower and lower price band than Intel. Intel's Pentium line spans the full range, from $100 to $500. The Pentium Pro models designed for desktops—those with 256K L2 caches—extend this range only slightly, mostly overlapping with the fastest Pentiums. Intel's 512K cache Pentium Pros, intended for servers, take the price points all the way up to more than $1,000.

Cyrix started its 6x86 campaign with prices quoted as "$1 more than Intel" on the assumption that the slightly higher performance offered by the Cyrix part enabled it to charge the same prices as Intel. This position didn't last long, however, as the company learned that to sway buyers away from Intel required not only a few percent higher perfor-
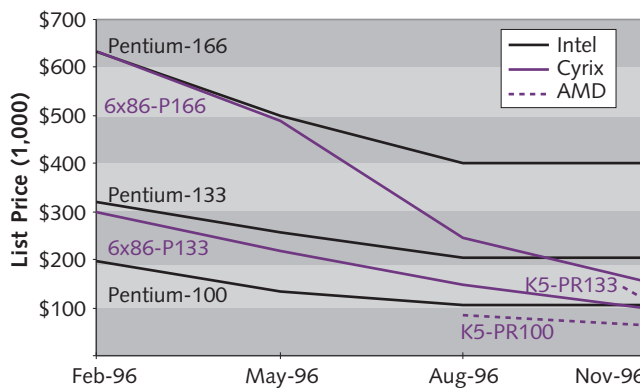

Figure 4. During 1996, Cyrix became much more aggressive in its pricing; AMD entered late, but with aggressive prices from the start. (Source: vendors)

mance but also steep discounts. Figure 4 shows how the price curves diverged in the summer. Cyrix's foundry and licensee, IBM Microelectronics, was the first to slash the 6x86 pricing, and Cyrix was forced to follow. The actual price spread between Intel and Cyrix parts is greater than shown in the figure because Cyrix discounts more heavily from its list price than Intel does.

AMD recognized from the start that it was late to market with parts with modest performance, and it priced its chips aggressively. Like Cyrix's, AMD's actual prices are likely to be well below the list prices shown in the figure.

Although Cyrix nominally began shipping the 6x86 months before AMD's K5, it was not until the third quarter that either part really began to ramp up. We estimate total shipments for the year to be around 1.7 million units for the K5 and 2.5–3 million units for the 6x86, divided between Cyrix and IBM Microelectronics. Many of these units were shipped near the end of the year; in the fourth quarter alone, Cyrix and IBM together shipped about 1.5 million units, and AMD shipped approximately 1 million units. Cyrix, IBM, and AMD combined captured about 7% of the Pentium-class market.

With an average selling price (ASP) below $100, AMD's total revenue from the K5 will be less than $150 million for 1996—far short of the cost of the company's x86 design teams and Fab 25, which is devoted to x86 processors. AMD also shipped about seven million 486 chips, which produced more revenue than the K5.

Cyrix's 6x86 achieved a higher ASP, thanks to its higher performance levels, enabling Cyrix to produce almost $200 million in revenue from the chip, with a similar amount earned by IBM Microelectronics. Note that Cyrix does not receive royalties from IBM's sales; as part of the foundry agreement, IBM is allowed to sell as many wafers full of Cyrix processors as it ships to Cyrix. (Cyrix signed a second agreement early this year that gives it access to additional wafers from IBM that are not part of the matching deal.)

Both companies need to dramatically increase their revenue next year to justify the investments they are making. Cyrix, having no other products, will live or die on the success of its x86 processors. AMD is a more diverse company, but it also has a much higher expense base for its x86 efforts.

Performance Positioning Becomes Challenging

In 1996, AMD and Cyrix both successfully used Pentium-equivalent clock speeds to position their products. Because the K5 and 6x86 both deliver greater performance than Pentium at a given clock speed, it is essential for these companies to move the focus away from clock speed, and the P rating achieved this. (Presumably due to legal pressure from Intel, AMD calls its rating the "PR" rating, but it has the same definition as Cyrix's P rating.)

The P rating was relatively simple to define and execute in 1996 because the processors were all pin-compatible and Intel had only one product line that AMD and Cyrix were

concerned with positioning against. In 1997, the situation will become dramatically more complex for several reasons. As Intel shifts to P55C, the P rating will become ambiguous; is a P200 relative to P54C or P55C?

Furthermore, both AMD and Cyrix will have chips faster than the fastest P55C. This makes it impossible to follow the method established for determining P ratings—comparing the performance of a system against one with the corresponding Intel processor. What will define the performance level associated with P233 or P266?

AMD and Cyrix will also want to position their fastest chips against Klamath as well as P55C. For this purpose, a "Klamath-equivalent clock speed" rating is needed, which is quite different from a Pentium-equivalent clock speed.

Another issue is what benchmarks to use for the performance ratings. In 1996, the P rating was based on Winstone 96, which is made up of integer business applications. This measure, or the newer Winstone 97, won't reflect performance on applications that use MMX, however, nor will it reflect the influence of floating-point performance on 3D games. It is inevitable that the performance positioning challenge will become more complex in the coming year; a single number just won't do the job in 1997.

Intel to Advance P6 Line Aggressively

We expect Intel to continue advancing the P6 product line at a rapid pace, constantly raising the bar for its competitors as well as the performance level of PCs. Table 3 summarizes the projected lineup. Klamath will be followed by Deschutes, which we expect to be little more than a shrink of the Klamath design to the 0.25-micron process. Deschutes should appear in late 1997 but isn't likely to be in volume production until 1998.

Following perhaps six months behind Deschutes is a more extensive enhancement of the Klamath design, called Katmai. We expect this chip to offer an extended version of MMX, as well as larger on-chip caches.

Willamette, which we expect in the second half of 1998, is rumored to be a next-generation derivative of the P6 core that presumably will offer additional execution units and instruction decoders to boost performance. Merced is the first implementation of IA-64, the new architecture codeveloped by Intel and Hewlett-Packard. Merced, which appears to have slipped into 1999, is likely to serve primarily the workstation and server markets, while Willamette drives high-end PCs.

Reshaping the Market in 1997

There is little doubt that Intel will hold the vast majority of the x86 market in 1997. At the same time, however, Intel's competitors should see significant growth, with a doubling or tripling of their modest 1996 share not unlikely.

For Intel, 1997 will be the year that the P6 family begins to take off. Even so, P55C will be the dominant part, since Klamath will be too expensive for the bulk of the market.

Name	Description	Availability
Klamath	P6 with MMX, external L2	2Q97
Deschutes	0.25-micron Klamath shrink	4Q97
Katmai	Enhanced with MMX2	1H98
Willamette (P68)	Next-generation x86	2H98
Merced (P7)	First IA-64 processor	1H99

Table 3. A guide to Intel's rivers—the code names used for Intel's P6-family of processors and beyond. (Source: MDR estimates)

Most important for Intel is that 1997 will set the stage for the P6 family to sweep the market in 1998.

Intel is likely to promote MMX heavily to drive the conversion to the new chips. Initially, there won't be much software that takes advantage of MMX, but many consumers will want it anyway—the fear of obsolescence is a powerful force. Three-dimensional graphics will be the driving force behind Klamath's move into the high-end consumer market.

In 1996, Cyrix took the lead in shipping Pentium alternatives. AMD is poised, however, to become the most significant alternate to Intel in 1997. At 8.8 million transistors, AMD's K6 is the most complex of the next-generation designs. Remarkably, it is also the smallest, at only 162 mm^2. With a compact, high-performance design, lots of fab capacity, strong sales and support, and multiple design teams, AMD should be in a strong position. This hasn't come cheaply: the company paid more than $600 million for NexGen and will invest more than $1 billion in Fab 25.

With what appears likely to be a slower chip that is later to market and without its own fab, Cyrix will have a tougher time. The lack of a fab potentially increases Cyrix's wafer costs and also increases the time needed to bring up a new design, since the turnaround time for new silicon is longer with a foundry. It also makes it difficult to tune the process for the chip designs. The combination of higher manufacturing costs and lower performance could put a crimp in Cyrix's ability to maintain adequate margins. A merger with another semiconductor maker is a distinct possibility.

New x86 Vendors to Appear

The coming year is likely to see at least one additional entrant into the x86 sweepstakes, with others to follow in 1998. Texas Instruments' long-awaited fifth-generation x86 core has been cancelled and TI is exiting the x86 business. Several startups are currently developing x86-compatible processors, however. Of these, the only acknowledged effort is from International Meta Systems, which has been working on x86-compatible designs for years. Other companies rumored to be working on chips that are x86-compatible include Rise Technology, Metaflow, and Transmeta.

All in all, 1997 should be an exciting year for the x86 microprocessor world. Intel's new processors and chip sets will trigger a new generation of PC designs, and Intel's dominance is well assured. AMD and Cyrix will have a long, hard struggle for market share, but for them 1997 is sure to be a lot better than 1996. Ⓜ