# PATENT WATCH

*by Rich Belgard, Contributing Editor*

*The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to* belgard@umunhum.stanford.edu.

## 5,539,911

*High-performance, superscalar-based computer system with out-of-order instruction execution*
Issued: July 23, 1996
Inventors: Le T. Nguyen, et al
Assignee: Seiko Epson
Filed: January 8, 1992
Claims: 56
A superscalar computer system with out-of-order instruction execution. The system has instruction buffering that includes two instruction buffers. Instructions are issued from the two instruction buffers.

## 5,537,656

*Method and apparatus for a microprocessor to enter and exit a reduced power consumption state*
Issued: July 16, 1996
Inventors: Thomas J. Mozdzen, et al
Assignee: Intel
Filed: June 17, 1994
Claims: 20
Method and apparatus for placing a microprocessor in and out of a reduced power-consumption state utilizing system interrupts: the microprocessor intercepts instructions executed by the processor before placing the processor in a reduced-power state. On a request for the processor to exit the reduced-power state, the method allows the processor to execute predetermined "resume" instructions to wait out any voltage-level fluctuations in the processor as it exits the reduced-power state and before allowing the processor to continue execution of the intercepted instructions.

## 5,535,348

*Block instruction*
Issued: July 9, 1996
Inventors: Jerald G. Leach, et al
Assignee: Texas Instruments
Filed: April 12, 1995
Claims: 3
A processor that contains a block-instruction handler. A block-start register is loaded with the beginning address of the block. A block-end register is loaded with the end instruction address, which is provided by the block instruction as a PC-relative value. A repeat counter is loaded with the repeat count. The block instruction is repeated multiple times.

## 5,535,397

*Method and apparatus for providing a context switch in response to an interrupt in a computer process*
Issued: July 9, 1996
Inventors: Richard J. Durante, et al
Assignee: Intel
Filed: June 30, 1993
Claims: 19
A processor that includes at least a pair of call stacks and a pair of register files that may be utilized for running processes. The processor switches between stack and registers to service an interrupt. The processor then runs an interrupt-start process that places the interrupted process into a condition in which the process may be safely interrupted. On interrupt completion, a corresponding context switch is made.

## 5,537,561

*Processor*
Issued: July 16, 1996
Inventor: Masaitsu Nakajima
Assignee: Matsushita
Filed: September 30, 1994
Claims: 8
A superscalar processor with multiple pipelines attaches tags to instructions in the decode unit to represent data dependencies and uses a pipeline-lock signal that may lock the pipelines based on the tags.

## 5,537,559

*Exception-handling circuit and method*
Issued: July 16, 1996
Inventor: James A. Kane, et al
Assignee: Meridian Semiconductor
Filed: February 8, 1994
Claims: 19
A circuit that monitors addresses generated by a microprocessor to check for address-exception conditions. Fetch-exception status bits are pregenerated for each instruction byte to indicate whether an address exception will be generated for each byte address. During fetch, the fetch-exception status bits are fed to an instruction buffer with the corresponding instruction bytes, where they are maintained until execution. Decode logic of an instruction-control unit analyzes the fetch-exception status bits upon execution and generates exceptions before the corresponding exception-causing instructions are executed.

## OTHER ISSUED PATENTS

**5,537,560** *Method and apparatus for conditionally generating a microinstruction that selects one of two values based upon control states of a microprocessor*
**5,537,538** *Debug mode for a superscalar RISC processor* M