PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,526,506

Computer system having an improved memory architecture
Issued: June 11, 1996
Inventor: Gilbert P. Hyatt
Assignee: None
Filed: September 4, 1990
Claims: 76
A system containing a processor, an address generator, an accessing unit, a memory, and at least one detector. The detector(s) detect(s) generated address characteristics, such as page-mode accesses. A detector may cause a delay in address generation based on characteristics of the memory addresses generated.

5,526,500

System for operand bypassing to allow a one-and-one-half-cycle cache memory access time for sequential load and branch instructions
Issued: June 11, 1996
Inventors: Darius F. Tanksalvala, et al
Assignee: Hewlett-Packard
Filed: February 10, 1995
Claims: 29
A pipeline structure that allows 1.5-cycle access time for both data and instruction caches. Half-cycle pulses allow execution of various instructions in half cycles. Data from a load instruction may be available for a subsequent instruction even though the access time for data cache is 1.5 cycles. Additionally, a branch address is available for a subsequent instruction even though the instruction-cache access time is 1.5 cycles.

5,524,262

Apparatus and method for renaming registers in a processor and resolving data dependencies thereof
Issued: June 4, 1996
Inventors: Robert P. Colwell, et al
Assignee: Intel
Filed: May 17, 1995
Claims: 5
A bypass mechanism within a register-alias table unit for handling source-destination dependencies between operands of a given set of operations issued simultaneously within a superscalar microprocessor.

5,524,224

System for speculatively executing instructions wherein mispredicted instruction is executed prior to completion of branch processing
Issued: June 4, 1996
Inventors: Marvin A. Denman, et al
Assignee: IBM, Motorola
Filed: June 30, 1995
Claims: 12
For a conditional branch instruction, the processor speculatively branches to the selected sequence of two or more possible target sequences before the system actually determines whether it is the correct sequence. If the system later determines the speculative branch is correct, processing continues. Alternatively, if the branch is wrong, the processor begins processing one or more correct instructions with a delay reduced from that of other systems.

5,524,222

Microsequencer allowing a sequence of conditional jumps without requiring the insertion of NOP or other instructions
Issued: June 4, 1996
Inventor: Mark W. Hervin
Assignee: Cyrix
Filed: November 22, 1994
Claims: 7
A sequencer for use in a pipeline architecture has circuitry for determining whether the previous instruction was a conditional jump and whether the condition was met, circuitry for determining whether the current instruction is a conditional jump, circuitry inhibiting a branch if the previous instruction was a conditional jump and the condition was met, as well as circuitry for treating a CALL instruction as a one-cycle unconditional jump if the preceding instruction was a conditional jump and the condition was not met.

5,524,221

Next-instruction pointer-calculation system for a micro computer
Issued: June 4, 1996
Inventors: Fumiki Sato, et al
Assignee: Mitsubishi
Filed: September 23, 1994
Claims: 4
An instruction decoder in a microcomputer for addressing instruction codes in a prefetch buffer, a field in a micro-ROM for storing the length of various instructions, and a position calculator in the bus-interface unit for inputting the number of words to indicate an address of instruction code in the prefetch buffer so the instruction code is read concurrently with the execution of the microinstruction. M