Cyrix Doubles 6x86 Performance with M2

MMX Added to Core; Larger Cache, Modified TLB Improve Scaling with Clock

by Michael Slater

Leveraging its 6x86 design, Cyrix is preparing a new chip based on the same core but with significantly improved caches and TLBs that enable the chip's performance to scale better as the clock speed increases. The new chip, described in detail for the first time at last week's Microprocessor Forum, also adds Intel-compatible MMX instruction-set extensions.

The past year has been a difficult one for Cyrix, as its 6x86—also called the M1—was delayed going into production, leaving a big hole between the decline of the company's 486 products and the rise of its Pentium-class line. Once the 6x86 achieved volume production this spring, the company encountered difficulty selling the chip, despite impressive performance and aggressive pricing. These difficulties resulted in poor financial results and the departure of some key employees, but company executives remain firm in their belief that major design wins are coming.

The M2 will build not only upon the 6x86 core, presumably enabling the chip to get to market more quickly, but also upon the customer development work that has been Cyrix's focus for much of this year. Being pin-compatible, it will also leverage the chip-set infrastructure (supporting a 75-MHz bus and linear burst mode) developed for the 6x86.

Cyrix expects the M2 to open up the notebook market as well. The current 6x86 is too power hungry for portables, although a version with a lower supply voltage could bring it into the portable range. For the M2, Cyrix added more power management, shutting off parts of the chip not in use. In addition, a more advanced process technology and lower supply voltage will cut the M2's power consumption.

Cyrix has just taped out the M2 design. Samples are promised by the end of this year, with production in 1H97. Cyrix has not disclosed the chip's formal name but will not call it the 7x86—a name presumably reserved for the next-generation M3.

Building on the 6x86 Core

Figure 1 shows the block diagram of the M2. The changes from the 6x86 fall primarily into two classes: enhancements to enable better scaling with clock speed and functional enhancements through instruction-set extensions.

The most obvious change is the quadrupling of the unified cache from 16K to 64K. As in the 6x86, a 256-byte instruction-line cache leaves the unified cache free for data accesses most of the time. As in the 6x86, the cache is four-way set-associative, has a 32-byte line size, and can perform two accesses per clock cycle.

A more subtle change is that the floating-point unit (which also implements the MMX instructions) now has its own dedicated bus to the cache instead of sharing the data path with the bus interface unit. In the 6x86, the FPU stalled if the bus interface was accessing the cache when the FPU request occurred; in the M2, both can access it concurrently.

The other change in the memory system is inside the memory-management unit. Cyrix's designers expected that the 128-entry TLB in the 6x86 would become a clock-speed limiter at higher frequencies. At the same time, traces of applications showed that TLB miss rates increased with 32-bit applications, making an even better hit rate important.

To achieve this goal, the M2 uses a two-level TLB. The relatively small, 16-entry level-one TLB is direct mapped to support high clock rates. It is backed by a 384-entry, six-way set-associative level-two TLB. The fast level-one TLB (with an estimated 92% hit rate) avoids the need for another pipeline stage for address translation during most accesses. When misses in the level-one TLB occur, an estimated 99.6% of accesses will hit in the level-two TLB and incur only a one-cycle penalty. Both TLBs are dual-ported to support both program and data address translations concurrently.

Few Core Enhancements

To reduce the number of stalls due to mispredicted branches, the number of entries in the branch target cache and branch

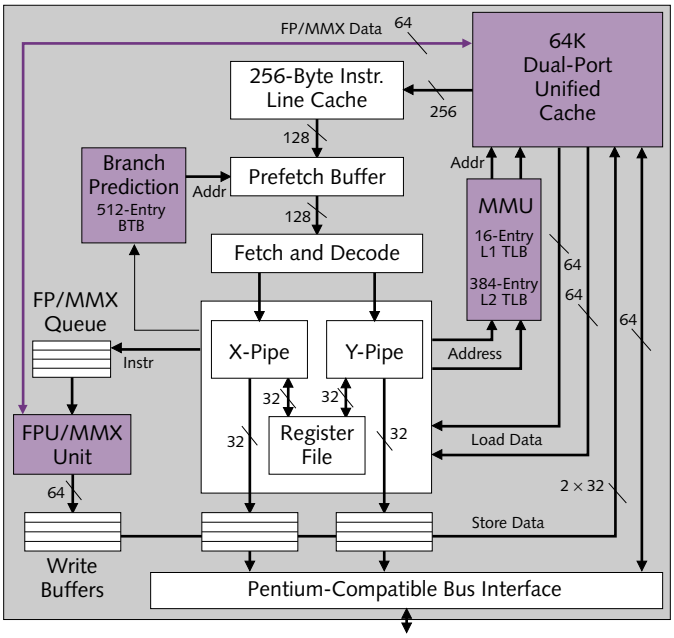


Figure 1. The M2 builds on the 6x86 core with four times as much cache, MMX extensions, a new TLB structure, and a larger BTB.

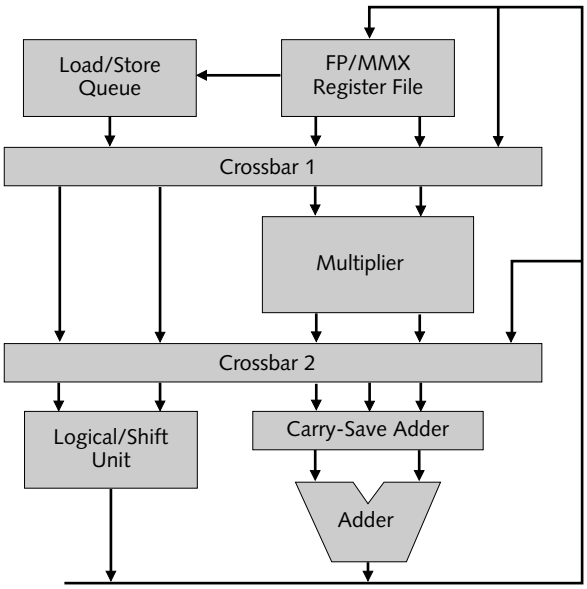


Figure 2. MMX operations are handled by the M2's FPU, which can deliver an MMX multiply-add result every clock cycle.

history table were doubled; each now has 512 entries. The organization and algorithms remain unchanged.

The pipeline is nearly identical to that in the 6x86, with the exception of MMX instructions (described later). As in the 6x86, the seven-stage pipeline is composed of an instruction-fetch stage, two stages for instruction decoding, two stages for address calculation, an execute stage, and a write-back stage *(see* **071401.PDF***)*.

Cyrix extended the 6x86 design to implement the full Pentium Pro instruction set. The new instructions include integer and floating-point conditional moves, floating-point compare, and reading from the performance-monitoring counters. The M2 identifies itself from the processor ID register as a type 6 (i.e., P6-family) processor.

One weakness of the 6x86 is that its floating-point unit is not as fast as Pentium's. In the M2, latencies of floating-point exchange, add, and multiply were cut by about a third. This should bring the chip closer to Pentium's FP performance, but it will still fall short of P6 performance.

	6x86	M2	P55C	Pentium Pro
L1 Cache	16K unified	64K unified	16K instr 16K data	8K instr 8K data
TLB	128-entry unified	16-entry L1 384-entry L2	32/64 (I/D)	32/64 (I/D)
BTB	256-entry	512-entry	256-entry	512-entry
Return Stack	8-entry	8-entry	4-entry	4-entry
Clock Ratios	1, 2, 3	2, 2.5, 3, 3.5	2.5, 3	2.5, 3
MMX?	No	Yes	Yes	No
Max Clock	150 MHz	225 MHz	200 MHz	200 MHz
Supply Voltage	3.3 V	2.5 V	2.5 V	3.3 V
Transistors	3 million	6 million	4.5 million	5.5 million
IC Process	0.44µ, 5M	0.33µ, 5M	0.28µ, 4M	0.35µ, 4M
Die Size	169 mm²	< 200 mm²	140 mm²	196 mm²
Est Mfg Cost*	$70	$85	$50	$145†

Table 1. The M2 adds enhancements to the 6x86 that take it well beyond the P55C. (Source: vendors, except *MDR estimates)

MMX Integrated Into FPU

Cyrix implemented the full MMX instruction set, based on Intel's public disclosure of the instruction set last spring. The company does not have any agreement with Intel regarding MMX and expects the patent license agreements held by its foundries (IBM and SGS-Thomson) to cover the MMX technology in the same way they cover the rest of the processor. One vulnerability is that Intel's actual implementation could differ, either intentionally or inadvertently, from the specifications the company has publicly disclosed.

Since the MMX register file is (as defined by Intel) aliased onto the floating-point register file *(see* **100301.PDF***)*, FP and MMX instructions cannot be intermixed. MMX instructions also share the 64-bit data width of the floating-point unit. As a result, it is natural to use the FPU data paths to implement the MMX operations. The multiplier and ALU were modified to support multiple subwords, saturating arithmetic, and multiply-add operations.

Figure 2 shows the FP/MMX unit block diagram in MMX mode. Operations that don't involve the multiplier are fed directly from crossbar 1 to crossbar 2, where they feed the other function units. During a multiply-add operation, operands pass through the multiplier in the first cycle, producing a partial sum and a partial carry. In the second cycle, these results are added, along with the third operand. The unit thus has a multiply-add latency of two clock cycles; because it is fully pipelined, it can deliver a new result every clock cycle.

Instructions are transferred to the FP/MMX unit during the execute stage of the basic pipeline. There is then an additional pipeline stage for accessing the FP/MMX registers, followed by one execute stage for arithmetic and logical operations or two stages for multiply and multiply-add operations. The final write-back stage makes a total of nine stages for arithmetic and logic operations and ten for multiply and multiply-add operations.

Cyrix added one proprietary feature to support multimedia software: cache-line locking. By locking critical software into the cache, the system can more easily guarantee its performance. Each cache line can be locked individually.

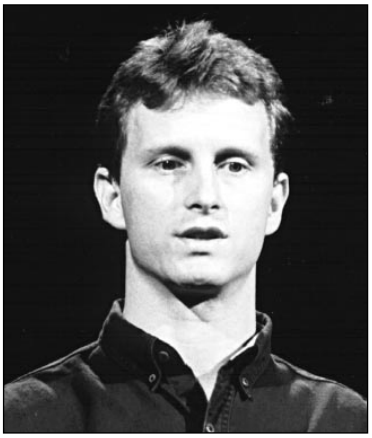
The cache-locking feature may be difficult to get software developers to use, however, since only the Cyrix processor will implement it. Unless Cyrix makes dramatic gains in market share, this feature is likely to sit idle in most systems. One possibility is that a system maker could provide an enhanced driver, or perhaps a video codec, that would use the cache-locking feature and deliver improved performance. This scenario is likely to occur only if Cyrix provides all the required software. Even if vendors use this feature, real-time application performance will be limited by the fundamental real-time weaknesses of Windows 95.

Clock Speed Reaches 225 MHz

Table 1 compares the key features of the 6x86, M2, and competitive processors. The M2's bus interface supports bus-to-core clock-speed multipliers of 2, 2.5, 3, and 3.5. Cyrix's initial offerings will all use a multiplier of 3 to deliver CPU speeds of 180, 200, and 225 MHz, with bus clocks of 60, 66, and 75 MHz. The 3.5 multiplier could support clock speeds up to 233 MHz with a 66-MHz bus or 262.5 MHz with a 75-MHz bus.

Cyrix's use of a 75-MHz bus gives its chip a potential advantage over Intel's P55C because of Cyrix's better bandwidth. Intel is likely to put its efforts behind Klamath and not push the P55C as far, while Cyrix (and AMD) must continue to extract more performance from the Pentium pinout. The 75-MHz processor bus requires the PCI bus to run asynchronously (or at 25 MHz), however, potentially reducing I/O performance. The "sweet spot" for the M2 is likely to be the 66/200-MHz version, but consumer demand for big numbers could make the 75/225-MHz part popular as well.

The M2 will be built using IBM's 0.33-micron five-layer-metal CMOS-5X process. SGS-Thomson also plans to build the chip but is likely to be many months behind IBM. The 6-million-transistor M2 runs from a 2.5-V core supply with 3.3-V I/O. Cyrix would not disclose the exact die size but said that it is under 200 mm^2.



MICHAEL MUSTACCHI

Cyrix's Michael Woodmansee describes the new features of the M2 at the Microprocessor Forum.

Equal to the Challenge?

Cyrix's goal for the M2 is to offer the industry's highest-performance x86 processor for Windows 95 and Windows NT desktop systems in 1997. So far, no benchmark results are available, making any objective evaluation impossible.

The larger caches and TLBs will demonstrate their worth at the large clock-speed multipliers that high core speeds require. As Intel's Pentium-200 shows, increasing the core clock speed beyond 166 MHz has relatively little payoff with a 16K cache. The M2's increased performance over the 6x86 comes from the combination of its higher clock speed and the cache and TLB enhancements. For a given bus speed, Cyrix estimates that an M2 running with a 3× multiplier will deliver about twice the application performance of a 6x86 running with a 2× multiplier.

Cyrix has promoted the 6x86's and M2's ability to run both 16- and 32-bit code efficiently as a key advantage over Intel's offerings, which push users toward Pentium for Windows 95 and Pentium Pro for Windows NT. This situation has caused confusion among PC buyers who want to start with Windows 95 but plan to move later to NT and can't decide which processor to select. Next year, Intel's positioning may be just as confusing, with the P55C wooing Windows 95 users and Klamath luring NT users. Cyrix might be able to take advantage of this confusion by promoting the M2 as the high-performance chip that lets you use either operating system with peak efficiency.

The reality, however, is that either of the Intel processors performs well with either operating system. Cyrix—which is perceived as a less stable supplier than Intel with a greater chance of having obscure problems in its chips—will find it hard to argue that it has the safer solution.

Intel's P55C should deliver greater MMX performance than the M2 because of its ability to dual-issue MMX instructions *(see* **101404.PDF***)*. Intel's multiply-add has a longer three-cycle latency but, as in the Cyrix design, is fully pipelined. Just how significant these differences are remains to be seen.

Cyrix positions the M2 as a competitor to Klamath as well as to P55C—just as it positioned the 6x86 as a competitor to Pentium Pro as well as to Pentium. The 6x86 did not, in fact, compete in the same market as Pentium Pro, and it was not competitive on 32-bit performance.

The M2 may fare better in comparisons with Klamath, although a final judgment must await performance measurements. Even if the M2 matches Klamath in integer performance, however, it will not match its FP performance or offer the same upgrade path as Klamath, nor will it work with Klamath chip sets—which will be the first to support AGP *(see* **100803.PDF***)*. Cyrix must hope that Pentium-bus chip sets with AGP become available in the same timeframe as Intel's AGP/Klamath chip set.

Cyrix will also face AMD's K6 *(see* **101406.PDF***)*. In some sense, it is AMD and Cyrix that are competing for those PC makers willing to use a non-Intel chip. Until measured benchmark results and pricing are available, meaningful comparisons between the two chips are very difficult to make. The K6 is a more complex design that allows greater out-of-order execution and has more execution resources, but, as the K5 showed, this technique doesn't always pay off.

If the M2 achieves its goals, Cyrix will be well positioned to continue its attempt to penetrate the PC microprocessor market. With a strong product and another year of experience under its belt, Cyrix should have a better year in 1997 than it had in 1996. M

Price & Availability

Pricing for the M2, which has not been formally announced, has not been disclosed. Samples are promised for late this year, with production in 1H97.

Contact Cyrix at 800.462.9749 or 214.968.8388, fax 214.699.9857, or access the Web at *www.cyrix.com*.