PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,513,330

Apparatus for superscalar instruction predecoding using cached instruction lengths
Issued: April 30, 1996
Inventor: David R. Stiles
Assignee: NexGen
Filed: October 27, 1993
Claims: 3
In a superscalar pipelined processor with variable-length instructions, circuitry is provided to determine the length of two instructions in parallel and align them. Parallel decoding circuitry is provided for decoding and executing the two instructions. A branch-prediction cache stores the target instruction and next sequential instruction and is tagged by the address of the branch instruction, as in the prior art. In addition, however, the branch-prediction cache also stores the length of the first and second instructions and the address of the second instruction. This additional data allows the target and next sequential instructions to be directly aligned and presented to the parallel decoding circuits without waiting for a calculation of their lengths and starting addresses.

5,511,212

Multiclock SIMD computer and instruction-cache enhancement thereof
Issued: April 23, 1996
Inventor: Todd E. Rockoff
Assignee: None
Filed: August 6, 1993
Claims: 24
A SIMD computer typically comprises one or more single-chip processing element (PE) modules, each having one or more PEs and interfaces to multichip subsystems (MCSs). The PEs are responsible for execution, while MCSs coordinate the PEs. One aspect of the invention augments the PE module with multiple clocks to regulate each PE and each MCS at its maximum rate. This invention gives the PE modules the ability to store and repeat instruction sequences at the highest possible rate within the PEs.

5,511,175

Method and apparatus for store-into-instruction-stream detection and maintaining branch-prediction-cache consistency
Issued: April 23, 1996
Inventors: John G. Favor, et al
Assignee: NexGen
Filed: October 20, 1994
Claims: 11
A branch-prediction cache (BPC) includes a tag identifying the address of branch instructions, a record of the last target of each branch instruction, and a copy of the first several instructions beginning at this target address. A separate instruction cache is provided for normal execution of instructions. The instruction cache monitors the system bus for attempts to write to the address of an instruction contained in the instruction cache. Upon such a detection, that entry in the instruction cache and in the BPC is invalidated.

5,509,130

Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor
Issued: April 16, 1996
Inventors: Richard D. Trauben, et al
Assignee: Sun
Filed: December 14, 1994
Claims: 12
A pipelined processor includes an instruction queue and an instruction-control unit to group and issue instructions in a single clock cycle for execution. Integer and floating-point function units capable of providing multiple results per clock cycle are also provided. The instruction queue stores sequential instructions of a program and target instructions of a branch instruction of the program, fetched from the instruction cache. The instruction-control unit decodes the instructions, detects operands cascading from instruction to instruction, and groups instructions.

5,509,129

Long instruction word controlling plural independent processor operations
Issued: April 16, 1996
Inventors: Karl M. Guttag, et al
Assignee: None
Filed: November 30, 1993
Claims: 117
A data processor that operates on instructions controlling multiple processor actions. Each instruction includes a data-unit section and an independent data-transfer section. The data-unit section includes a data-operation field that indicates the type of arithmetic-logic-unit operation and six operand fields. The six operand fields include four source-data register fields and two destination-register fields. The data unit includes a multiplication unit and an arithmetic logic unit. The data unit may include a barrel rotator for one input of the arithmetic logic unit. M