PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu

5,495,617

On-demand powering of necessary portions of execution unit by decoding instruction word field indications which unit is required for execution [sic]
Issued: February 27, 1996
Inventor: Kouichi Yamada
Assignee: NEC
Filed: June 2, 1995
Claims: 11
A CMOS microprocessor with an instruction decoder and a second decoder that applies a standby control signal to the execution unit if it is not used.

5,495,590

Checkpoint synchronization with instruction overlap enabled
Issued: February 27, 1996
Inventors: Steven T. Comfort, et al
Assignee: IBM
Filed: June 7, 1995
Claims: 6
A processor that can isolate errors to an interval between checkpoints, allowing instructions to overlap. Checkpoints are established before and after certain instructions, and all processing from before a checkpoint must be done before instruction completion. Instructions from beyond a checkpoint are allowed to be processed up to the point of completion (but no farther) while waiting for the checkpoint to be cleared.

5,493,687

RISC microprocessor architecture implementing multiple typed register sets
Issued: February 20, 1996
Inventors: Sanjiv Garg, et al
Assignee: Seiko Epson
Filed: July 8, 1991
Claims: 5
This register system for a multimode processor provides multiple identical banks of register sets, to which the processor controls access such that instructions do not specify the given bank. An integer register set includes first and second subsets and a shadow subset of the second set. While the processor is in a first mode, instructions access the first and second subsets. In the second mode, instructions may access the first subset, but any attempts to access the second subset are transparently rerouted to the shadow subset instead, allowing system routines to seemingly use the second subset without having to save and restore data that user routines have written to the second subset.

5,493,684

Power-management architecture including a power-management messaging bus for conveying an encoded activity signal for optimal flexibility
Issued: February 20, 1996
Inventors: Douglas D. Gephardt, et al
Assignee: AMD
Filed: April 6, 1994
Claims: 17
A microprocessor includes a CPU core coupled to a variety of on-chip peripherals. The microprocessor also has a power-management message unit (PMMU) coupled to the peripherals for monitoring the internal interrupt and bus request signals of the microprocessor. Based on the detected activities, if any, the PMMU sends a message on a power-management message bus to an external power-management unit. Power-management decisions are made by the external power-management unit as to the appropriate power-management mode to enter. The PMMU controls the frequencies of the CPU clock signal and a system clock signal; it may also control power to various external peripheral devices

5,493,669

Data processor for simultaneously searching two fields of the rename buffer having first and second most recently allocated bits
Issued: February 20, 1996
Inventor: Marvin A. Denman, Jr.
Assignee: Motorola
Filed: March 3, 1993
Claims: 2
A data processor has multiple execution units, a rename buffer coupled to at least one of the execution units, and architectural registers coupled to at least one execution unit and to the rename buffer. The rename buffer receives and stores results and receives requests for operands. Each received result and operand is associated with an architectural register. The rename buffer periodically forwards one of a set of received results to an execution unit. Each received result of the set is associated with the same architectural register. The rename buffer can determine which entry is the most recently allocated among several that will update the same architectural register.

OTHER ISSUED PATENTS

5,493,683 *Register for identifying processor characteristics*
5,493,667 *Apparatus and method for an instruction cache locking scheme* M