PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu

5,487,156

Processor architecture having independently fetching, issuing, and updating operations of instructions which are sequentially assigned and stored in order fetched
Issued: January 23, 1996
Inventors: Valeri Popescu, et al
Assignee: same
Filed: December 5, 1990
Claims: 36
A processor architecture that uses a dynamic register file to decouple instruction fetch from execution functions. The instruction fetch operates in a free-running mode that does not stop if a fetched instruction cannot be executed due to data or instruction dependencies. Branch instructions are predicted, and the results of execution of all instructions are provisionally stored pending validation or invalidation on the basis of the dependencies becoming available later.

5,481,751

Apparatus and method for storing partially-decoded instructions in the instruction cache of a CPU having multiple execution units
Issued: January 2, 1996
Inventors: Donald B. Alpert, et al
Assignee: National
Filed: October 17, 1994
Claims: 2
A microprocessor partially decodes instructions retrieved from main memory before placing them into the microprocessor's integrated instruction cache. Each storage location in the instruction cache includes two slots for decoded instructions. One slot controls one of the microprocessor's integer pipelines and a port to the microprocessor's data cache. A second slot controls the second integer pipeline or one of the microprocessor's floating-point units. The instructions retrieved from main memory are decoded by a loader unit that decodes the instructions from the compact form as stored in main memory and places them, along with auxiliary control information, into the two slots of the instruction cache entry according to their functions.

5,481,693

Shared register architecture for a dual-instruction-set CPU
Issued: January 2, 1996
Inventors: James S. Blomgren, et al
Assignee: Exponential Technology
Filed: July 20, 1994
Claims: 7
A dual-instruction-set central processing unit (CPU) is capable of executing instructions from a RISC instruction set and a CISC instruction set. Data and address information may be transferred from a CISC program to a RISC program running on the CPU by using shared registers. The condition code and general-purpose registers (GPRs) are merged together, allowing a CISC program to pass data to a RISC program merely by writing one of its GPRs and switching control to the RISC program.

5,481,686

Floating-point processor with apparent-precision-based selection of execution precision
Issued: January 2, 1996
Inventor: Kenneth Dockser
Assignee: VLSI
Filed: May 4, 1995
Claims: 7
A floating-point processor with an input-format converter, operand registers, a mode selector, an execution unit, and a result-format converter. The FPU performs operations in their apparent precision, defined as the smallest precision in which the number will fit without loss of accuracy, rather than their specified precision. The results are stored in extended precision regardless of the execution precision.

5,481,683

Superscalar computer architecture using renamed and recycled general-purpose registers to manage out-of-order execution of instructions
Issued: January 2, 1996
Inventor: Faraydon Karim
Assignee: IBM
Filed: March 19, 1993
Claims: 17
A superscalar computer architecture executes instructions out of order while managing data dependencies and maintaining precise interrupts. Multiple registers and tables rename and recycle source and destination addresses referenced to a general-purpose register. Access to destination data in the general-purpose register is locked until the instruction associated with the data is fully executed.

OTHER ISSUED PATENTS

5,488,730 *Register-conflict scoreboard in pipelined computer using pipelined reference counts*
5,488,729 *Central-processing-unit architecture with symmetric instruction scheduling to achieve multiple instruction launch and execution*
5,475,856 *Dynamic multimode parallel processing array* M