SiS Rolls Out Pentium, PPro Chip Sets

Trinity, Archer, Genesis Create New Levels of Integration

by Linley Gwennap

Silicon Integrated Systems (SiS) is preparing to let loose over the next few months a barrage of new chip sets that will reduce the cost of Pentium and Pentium Pro systems by shrinking the number of system-logic chips. The rollout begins with Genesis, a mainstream chip set that is the first to combine Pentium system logic and a graphics accelerator in a single chip. It will be followed by Trinity, a high-performance chip designed for more expensive Pentium systems, and Archer, the first single-chip system-logic solution for Pentium Pro. Already shipping more system-logic chip sets than any vendor other than Intel, SiS is keeping the pressure on its competitors with its rapid introductions.

Genesis Eliminates Graphics Subsystem

Taking the unified memory architecture (UMA) one step further, Genesis eliminates not just the graphics frame buffer but the entire graphics subsystem as well. Although others have implemented UMA designs, the Genesis device is the first to integrate a 64-bit 2D graphics accelerator with the main-memory controller on a single chip. This chip, along with an ISA bridge and a Super I/O chip, provides all the logic needed for a basic Pentium PC, as Figure 1 shows.

SiS has simply combined its 5511/5512 chip set with its 6205 graphics accelerator to form the core of Genesis (5596). A move to 0.5-micron CMOS helped enable the integration.

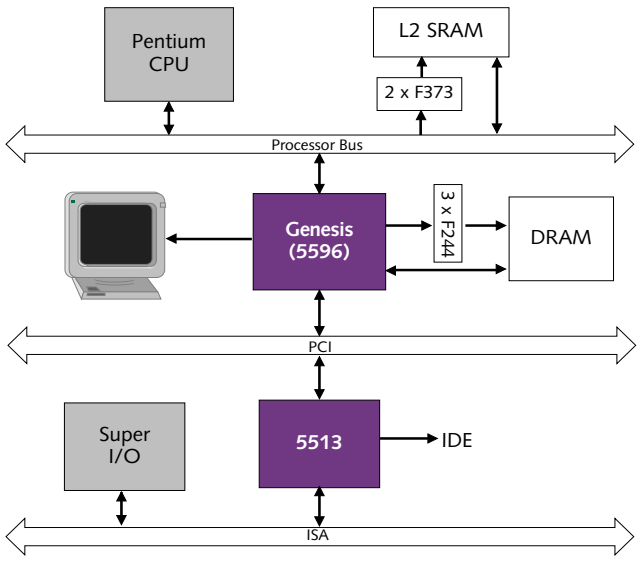

Figure 1. Genesis (5596) provides Pentium system logic plus a 2D graphics accelerator in a UMA configuration. A separate ISA bridge (5513) is required to complete the system.

To handle the high pin-out requirements, Genesis uses a high-density BGA package with 388 leads. A separate PCI-to-ISA bridge (5513) is needed for ISA compatibility and basic PC peripherals.

In a UMA design, the frame buffer is stored in main memory, creating contention between graphics and CPU accesses. To ease this contention, Genesis compresses the data in the frame buffer to reduce the memory bandwidth needed for screen refresh, a technique used by other UMA designs *(see* **090801.PDF** *)*. SiS believes its algorithm will achieve about a 6:1 compression ratio, reducing refresh bandwidth by more than 80%. Performance is further improved due to the close coupling of the graphics accelerator with the system logic, eliminating some overhead.

The graphics accelerator provides the basic 2D functions that have become a commodity in today's market. In addition to GUI acceleration, Genesis supports scaling and color-space conversion for video acceleration; it even sports a proprietary "feature port" that connects to the SiS 6204, for video overlays. Both the RAMDAC and clock generator are integrated; the chip connects directly to the monitor. Performance should be comparable to that of other fast DRAM-based 2D accelerators.

The system logic is also adequate for a mainstream system. It supports fast-page-mode and EDO DRAM and takes only five cycles to access the first quadword. The cache can be as large as 1M with asynchronous, burst, or pipeline burst (PB) SRAM. Genesis complies with the DPMS power-management standard and Plug-and-Play standard. The PCI interface supports concurrent and delayed transactions, as in the PCI 2.1 specification; with these features, PCI performance should be similar to that of Intel's latest chip set, Triton II *(see* **1002MSB.PDF** *)*.

Despite the high level of integration, several external TTL chips are required to complete the system. Figure 1 shows the two F373s needed to latch the L2 cache address as well as the three F244s that buffer the DRAM address. For systems that use the XD bus to support a BIOS ROM or keyboard controller, a sixth TLL chip is needed to decouple the XD bus from the ISA bus.

The Genesis chip set lists for $39 in quantities of 1,000. With Intel selling its 440VX (Triton II) chip set for $33, SiS is essentially offering 2D graphics acceleration for just $6.

The low price and UMA design of Genesis allow system vendors to build very low cost Pentium PCs. A bare-bones configuration would include an L2 cache and 8M of main memory. But because Windows 95 runs poorly in less than 8M, and the UMA design requires a portion of the main memory for the frame buffer, a better configuration would

include no L2 cache and 16M of EDO DRAM. With the recent drop in DRAM prices, this configuration would add about $60 to the build cost while delivering performance near that of non-UMA systems.

Trinity Integrates ISA Interface

For high-end systems, SiS has taken a different tack. The Trinity (5571) chip must be coupled with a separate graphics subsystem, as Figure 2 shows. Separating the frame buffer from the main memory improves performance and allows PC makers the flexibility to add a high-end 2D or 3D graphics accelerator. Instead of integrating the graphics controller, Trinity combines the so-called north bridge and south bridge of a typical Pentium chip set into one component.

Trinity's system-logic feature set is similar to that of Genesis, with a few key improvements aimed at increasing performance. Trinity adds support for burst EDO and synchronous DRAM for single-cycle (X-1-1-1) burst reads. Only PB SRAM is allowed; with prices for these parts dropping, this restriction is reasonable for a high-end chip set. Like Genesis, Trinity supports concurrent and delayed PCI transactions for high PCI performance.

Trinity contains a complete PCI-to-ISA bridge based on the company's 5513 chip. In addition, it supplies the traditional DMA controller, interrupt controller, real-time clock, and keyboard controller. It adds support for flash BIOS and two USB ports. To contain all this I/O, Trinity, like Genesis, uses a BGA package, but it requires 480 leads.

SiS plans to sample Trinity in June, with volume production in 3Q96. Pricing is $29 in 1,000s, making it competitive with Intel's 430VX chip set, which lists for $33. Trinity's feature set is very similar to that of the 440VX; with EDO DRAM, Trinity is actually one cycle faster than the Intel chip set, offering a small potential performance advantage.

SiS, Intel Divide Market Differently

With its 430VX and 430HX (Triton II) chip sets, Intel has targeted consumer and business systems, respectively. In each of these segments, however, Intel offers a single chip that spans low-end to high-end systems. SiS instead divides the market between low-cost systems (Genesis) and high-performance systems (Trinity), using the same chip sets for both consumer and business systems.

For low-end systems, Genesis offers a potential cost advantage over the Intel chip sets due to its integrated graphics controller. Genesis requires a UMA design, however, which in turn requires 16M of main memory for reasonable performance. In 8M configurations, systems using Triton II in a non-UMA arrangement will far outperform Genesis-based systems but will cost significantly more. In 16M configurations, which will become more popular in 2H96, Genesis retains the same cost advantage and could close most of the performance gap.

Trinity matches up well against the 430VX for high-performance systems while offering cost and board-space advantages. The SiS chip set can also be used for business systems, matching the key features of the 430HX as well. Trinity's only shortcoming compared with the 430HX is a lack of support for parity or ECC main memory, but this feature is used in only a few high-end PC servers and is not needed for the mainstream business market.

Price & Availability

Although early versions of the Genesis chip set (SiS 5596 and 5513) are sampling now, the version described here will sample in June with volume production planned for July. The list price for the two-chip set is $39.

SiS plans to sample Trinity (SiS 5571) in June, with production in 3Q96. Both samples and production of Archer (SiS 5601) are expected in 3Q96. Trinity lists for $29, while Archer sells for $39. All prices are in quantities of 1,000.

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Archer Aims for P6 Systems

Completing the onslaught is a chip called Archer (5601), the first P6 chip set from SiS and the first single-chip design for the P6. While SiS becomes the third (and certainly not the last) vendor to introduce a P6 chip set, this level of interest is not due to Pentium Pro—that processor will sell only a few million units this year, with the vast majority placed on Intel motherboards. These chip-set makers are positioning themselves for 1H97, when Intel is expected to deploy Klamath, a lower-cost version of the P6 that uses the same system bus as Pentium Pro. We use the term P6 chip sets for products that

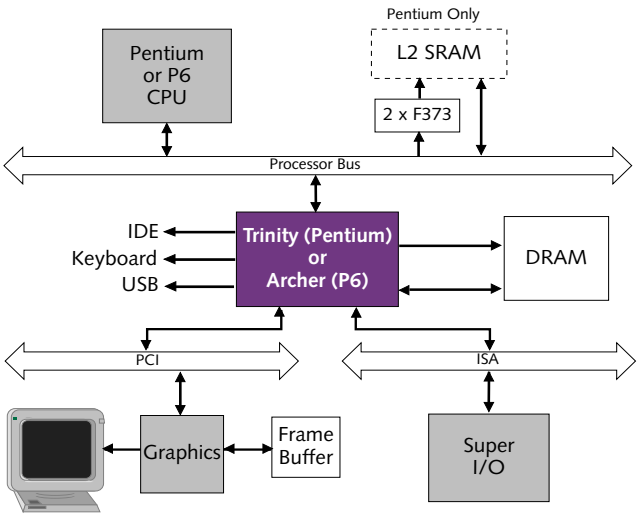

Figure 2. Trinity (5571) combines Pentium system logic and an ISA port into a single device. Archer (5601) provides the same feature set for a P6 system. A separate graphics subsystem is required.

support the expected range of P6-family processors, all using the same P6 bus.

From an integration standpoint, Archer is nearly identical to Trinity, providing connections to the processor bus, main memory, PCI, ISA, and USB, as Figure 2 shows. Unlike Trinity, Archer need not control the L2 cache; in a P6 system, this function is handled by the processor. Like Trinity, Archer uses a 480-lead BGA.

The key difference between Trinity and Archer is, of course, the processor-bus interface. Archer is compatible with the split-transaction P6 bus *(see* **090701.PDF** *)*, including the proper GTL+ voltage levels. The chip can accept data at the full rate of the bus, using an eight-entry write buffer (with each entry a full 32-byte cache line) to avoid stalling the processor.

Archer takes advantage of the "deferred reply" feature of the P6 bus on reads from PCI. Because these reads take many CPU cycles to complete, Archer accepts the read but releases the pipelined P6 bus for other traffic. Once the PCI read completes, Archer will rearbitrate for the bus and direct the data to the requesting CPU.

Intel's latest P6 chip set, the 440FX *(see* **100604.PDF** *)*, requires three chips to perform the same functions as the single-chip Archer. Partly for this reason, the 440FX lists for more than twice the price of the $39 Archer. In most configurations, Archer should deliver performance similar to that of the Intel chip set.

Archer does not offer the same expandability as Intel's chip sets, however. It allows only a single processor, while the 440FX handles two and its big brother, the 450GX, supports four. Archer supports up to 512M of parity or ECC memory, but the 440FX can double that amount. Although the Intel chip sets may be favored for high-end servers and workstations, for desktop PCs Archer's capabilities should be more than adequate.

Complete Makeover for SiS

The new products from SiS display a creativity that will be required for chip-set makers to stay in business. Instead of copying Intel's features and system partitioning, SiS has created a set of highly integrated devices that should reduce the cost and size of both Pentium and Pentium Pro systems. The key enablers are dense 0.5-micron technology, high-pin-count BGA packages, unified memory architecture, and the company's experience with graphics as well as system logic.

With this round of product introductions, SiS is setting the pace for condensing Pentium and P6 system logic into a single chip. With the fast product cycles in the chip-set market, however, other chip-set vendors will probably deploy similarly integrated products in the next 6–12 months.

Genesis' combination of graphics and system logic affirms another trend. With even Intel moving into the graphics area *(see* **1007MSB.PDF** *)*, it is clear that chip-set vendors without graphics expertise (and vice versa) will find rough going in the future. MR