PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,471,626

Variable-stage entry/exit instruction pipeline
Issued: November 28, 1995
Inventors: Michael J. Carnevale, et al
Assignee: IBM
Filed: May 6, 1992
Claims: 17

An instruction pipeline includes a sequence of pipeline stages, each dedicated to one of several operations. Control words control execution of operations as they progress through the pipeline. The pipeline stages, as well as pipeline entry and exit, are interconnected in a way that permits each control word to enter and exit the pipeline at any stage, and to skip any stages in which the control word does not control any operations. On occasion, this permits a control word to pass another control word that originally preceded it in the pipeline, thereby reversing the order of the two control words. A mapping field in each control word predetermines its route through the instruction pipeline, one bit of the map field corresponding to each pipeline stage. The route of each control word is also controlled by arbitration logic to resolve contention among control words for particular pipeline stages, and to ensure against incorrect out-of-order execution.

5,471,598

Data dependency detection and handling in a microprocessor with write buffer
Issued: November 28, 1995
Inventors: Marc A. Quattromani, et al
Assignee: Cyrix
Filed: October 18, 1993
Claims: 6

In a superscalar superpipelined microprocessor having a write buffer located between the core and cache, the buffer is controlled to store the results of write operations to memory until the cache becomes available. The write buffer includes multiple entries that are split into two circular buffer sections for facilitating the interaction with the two pipelines of the core; cross-dependency tables are provided for each write-buffer entry to ensure that the data is written from the write buffer to memory in program order. Other features, including noncachable reads, handling speculative execution, detecting and handling data dependencies and exceptions, and performing special write functions (misaligned writes and gathered writes), are also given.

5,471,593

Computer processor with an efficient means of executing many instructions simultaneously
Issued: November 28, 1995
Inventor: Michael H. Branigin
Filed: January 21, 1994
Claims: 12

In a pipelined processor, conditional instructions are issued and executed, including branches and others, before the controlling conditions may be available. Conditional instruction execution is also improved by a condition-code mask field in instructions to choose the condition-code bits involved in the decision; by a flag to enable or disable the setting of a condition code; by stale condition-code handling to determine if the logically previous conditionally executing instruction was successful in setting the condition code and to conditionally execute accordingly; by multiple condition codes, so independent instruction sequences can use condition codes in parallel; and by condition-code reservation stations to capture a condition code as soon as it becomes available and hold that value until needed, thus freeing the condition code as soon as possible for use by other instructions.

5,471,591

Combined write-operand queue and read-after-write dependency scoreboard
Issued: November 28, 1995
Inventors: John H. Edmondson, et al
Assignee: Digital
Filed: October 30, 1992
Claims: 18

In a pipelined digital computer, an instruction decoder decodes register specifiers from multiple instructions and stores them in a source queue and a destination queue. An execution unit successively gets source specifiers of an instruction from the source queue, initiates an operation upon the source specifiers, reads a destination specifier from the destination queue, and retires the result at the specified destination. Read-after-write conflicts may occur because the execution unit may overlap execution of multiple instructions. Just prior to beginning execution of a current instruction, the destination queue is checked for conflict between the source specifiers of the current instruction and the destination specifiers of previously issued but not yet retired instructions. When an instruction is issued for execution, its destination specifiers in the destination queue are marked to indicate that they are associated with an executed (but not yet retired) instruction.

OTHER ISSUED PATENTS

5,471,602 *System and method of scoreboarding individual cache line segments* M