GLANCE A T

New Embedded CPU Goes ShBoom

Patriot Scientific's PSC1000 is the first device to implement the ShBoom architecture, an unusual stack-based instruction set. By operating mainly on the top of stack, the instructions avoid operand specifiers, allowing them to fit into 8 bits. These tiny instructions in turn reduce code space. At \$20 and about 20 Dhrystone MIPS, the chip sets no price/performance records; Patriot believes the stackbased design will perform well on Java applications, however. The company expects to sample the PSC1000 in the next few months.

Intel's pace of product introductions will slow in the coming months, with nothing much planned before the introduction of the P55C late this year. As the Pentium family nears maturity, Intel's average selling price (ASP) for PC processors is falling, causing revenue growth to slow. The introduction of new P6-family parts in 1997, however, will raise both the ASP and revenue growth.

1

HP grabs performance lead; Digital developing low-cost 21164; Cyrix PCs debut; AMD advances Elan with SC310; AGP to provide new graphics connection; 3DO licenses technology to Cirrus; Intel delivers docking chips.

Intel's i960 Loses Its Luster 11

Once the leader in 32-bit embedded RISC sales, the i960 has fallen to number two in 1995 and is likely to be no better than third in 1996. The company's initial success was in laser printers, but this market is maturing while the growth is coming from emerging consumer devices such as video games. Intel's current products are too expensive and power-hungry for these consumer devices, locking them out of these design wins. Intel is scrambling to reposition its i960 line, but it looks like the company may be too late to ride the wave of new consumer products.

Viewpoint: Java Virtual Machine Should Stay Virtual. 14 Sun Microelectronics has proposed a plan to build microprocessors that directly execute the Java instruction set. Brian Case points out that this plan has many drawbacks and should be scrapped. Java runs just fine on general-purpose processors using just-in-time

compilation techniques, whereas a Java chip would be unable to execute non-Java code. Thus, the volume of Java chips is likely to be far smaller than that of general-purpose devices, and economies of scale will hamper the Java chips. A better approach would be to enhance a standard processor core with a few Java acceleration instructions.

Literature Watch	16
Recent IC Announcements	17
Patent Watch	18
Chart Watch	19
Resources	20

Publisher and Editorial Director Michael Slater E-mail: mslater@mdr.zd.com

> Editor in Chief Linley Gwennap E-mail: linley@mdr.zd.com

Senior Editor Jim Turley E-mail: jturley@mdr.zd.com

Senior Analyst Yong Yao E-mail: yyao@mdr.zd.com

Editorial Assistant: Suzanne Gifford

Editorial Board

Dennis Allison Brian Case John Novitsky Nick Tredennick

Rich Belgard Dave Epstein Bernard L. Peuto John F. Wakerly

Editorial Office 480 San Antonio Rd., Suite 210 Mountain View, CA 94040 Phone: 415.917.3050 Fax: 415.917.3093

Microprocessor Report is published every three weeks, 17 issues per year. Rates are: N. America: \$495 per year, \$895 for two years. Europe: £375 per year, £645 for two years. Elsewhere: \$595 per year, \$1,095 for two years. Additional copies in the same envelope: \$175 per year in North America, \$225 elsewhere. Back issues are available.

> Published by MicroDesign RESOURCES

President: Michael Slater

Business Office 874 Gravenstein Hwy. So., Suite 14 Sebastopol, CA 95472 Phone: 707.824.4004 Fax: 707.823.0504 Subscriptions: 707.824.4001 E-mail: cs@mdr.zd.com

World Wide Web: www.chipanalyst.com

Copyright ©1996, MicroDesign Resources. All rights reserved. No part of this newsletter may be reproduced, stored in a retrieval system, or transmitted in any form or by any means without prior written permission.

Winner, Computer Press Award, 1993, 1994

