PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments via e-mail to belgard@umunhum.stanford.edu

5,467,460

M&A for minimizing data transfer to main memory from a writeback cache during a cache miss
Issued: November 14, 1995
Inventor: Piyush G. Patel
Assignee: Intel
Filed: April 28, 1994
Claims: 4
A cache memory having at least two modified bits for each block of data coupled to a writeback buffer circuit for transferring a fraction of the data block when a cache miss occurs. The data array of the data cache is partitioned into two halves; each block of data has two dirty bits. When a cache miss occurs, a replacement algorithm determines which of the lines in a given set shall be replaced. The contents of the chosen line in the data cache is copied to a writeback buffer circuit. The line of data from external memory is then written into the data cache, clearing the two dirty bits in the data cache in the process. If only one dirty bit is set, only half of a block of data is written back into the data cache.

5,467,455

Data-processing system and method for performing dynamic bus termination
Issued: November 14, 1995
Inventors: James G. Gay, et al
Assignee: Motorola
Filed: November 3, 1993
Claims: 29
A data-processing system and a method for performing dynamic bus-signal termination uses a dynamic bus-termination circuitry with a device. The circuitry is enabled when data is incoming to the device and is disabled when data is outgoing from the device to selectively reduce unwanted signal reflection at the signal end of a bidirectional bus. The disabling allows the circuitry to be removed or tristated from any connection with the bus when not needed (i.e., data outgoing) to reduce loading. The disabling of the termination circuitry also aids in reducing the power consumption of the part when either the bus is sitting idle or the part is in a low-power mode of operation.

5,465,373

Method and system for single-cycle dispatch of multiple instructions in a superscalar processor system
Issued: November 7, 1995
Inventors: James A. Kahle, et al
Assignee: IBM
Filed: January 8, 1993
Claims: 7
A method and system for permitting single-cycle instruction dispatch in a superscalar processor system that dispatches multiple instructions simultaneously to a group of execution units for execution and storing of results. Multiple intermediate storage buffers are provided, and each time an instruction is dispatched to an available execution unit, one of the intermediate storage buffers is assigned to any destination operand within the dispatched instruction, permitting the instruction to be dispatched within a single cycle by eliminating any requirement for determining and selecting the register.

5,465,336

Fetch and store buffer that enables out-of-order execution of memory instructions in a data-processing system
Issued: November 7, 1995
Inventors: Benjamin T. Imai, et al
Assignee: IBM
Filed: June 30, 1994
Claims: 2
A method and device for handling fetch and store requests in a data-processing system. A fetch and store buffer consists of a store queue, a fetch queue, a register, a comparator, and a controller. The store queue and the fetch queue receive requests from one or more execution units. When the fetch queue receives a fetch request from an execution unit, it sets a mark in a field associated with the request, indicating the store queue entries present at the time the fetch request is entered. It then removes the mark from the field when the associated store queue entry is drained.

The controller sends a queued fetch request to the memory unit when it is ready to accept a request. The comparator determines if there is a dependency between the request in the memory unit address register and any store queue entries marked in the gated request's field. When a dependency is determined by the comparator, the controller drains the store queue entries marked in the pending fetch request's field from the store queue prior to draining the fetch queue entries.

OTHER ISSUED PATENTS

5,469,547 *Asynchronous bus interface for generating individual handshake signal for each data transfer based on associated propagation delay within a transaction*
5,467,318 *Address generating and decoding apparatus with high operation speed*
5,465,377 *Compounding preprocessor for cache for identifying multiple instructions which may be executed in parallel* M