# Motorola, TI Extend 16-Bit DSP Families

## *568xx, 320C2xx Girded for Battle over High-Volume Applications*

*by Jim Turley and Phil Lapsley*

Two new DSP families from Texas Instruments and Motorola are prepared to capture a large chunk of the growing 16-bit DSP market. Almost simultaneously, the two vendors revealed plans to dramatically lower the price of midrange fixed-point DSP performance to under $10 in volume. While Motorola focuses on ease-of-use and programmability, TI provides a compatible growth path including on-chip RAM, ROM, and—for the first time—flash memory.

### Motorola 56800 Borrows from 56100

Hot on the heels of its high-end 56300 announcement *(see* **091605.PDF***)*, Motorola revealed its new low end, the 56800 family. These new 20-MIPS DSPs are interesting primarily because of their programming model. The 56800 is a hybrid of a DSP and a traditional 16-bit microcontroller. The chips should integrate easily into control-oriented applications by providing a number of on-chip peripheral functions that microcontroller users have come to expect.

Digital signal processors have become less of a boutique item and more widespread, fostering a need to combine DSP cores with conventional microcontrollers. The combination provides true signal-processing capability with control-oriented functions normally associated with microcontrollers. The company is targeting control-oriented applications in answering machines, motor control, automotive noise suppression, and portable communicators.

The 56800 borrows heavily from its architectural predecessor, the 56100, but makes a number of changes. The two core designs share a similar overall architecture and internal data paths, but the 56800 family has fewer registers. As Figure 1 shows, the 56800 core has three 16-bit general-purpose data registers, whereas the 56100 has four, and only one address-modifier and one offset register in place of a set of eight. The 56800 enlarges its program counter to 19 bits, up from the 56100's 16 bits.

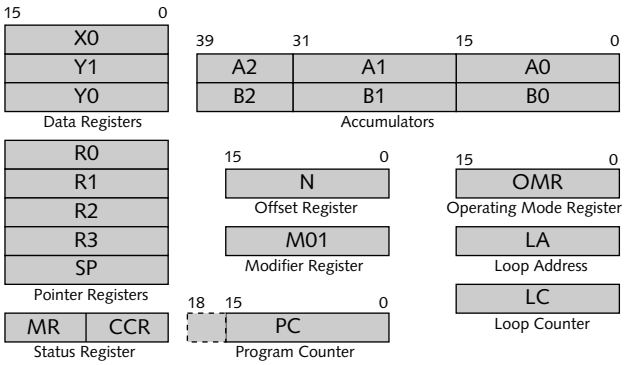


**Figure 1.** The 56800 retains the 56100's 40-bit accumulator registers but drops one general-purpose data register. The 56800's program counter was extended to 19 bits for a bigger code space.

### New Design Appeals to CPU Programmers

By reducing and rearranging the register set, Motorola was able to encode the 56800's instructions more efficiently. One benefit programmers will applaud is the ability to reference memory-resident operands rather than adhering to a strict load/store model. The instruction set is also considerably more orthogonal, with few of the irregular register restrictions of the 56100. All in all, the instruction set looks more like that of a good 16-bit microprocessor than that of a DSP.

The 19-bit program counter aids applications that exceed 64K words of code. The most significant three bits are stored in the chip's status register, allowing a simple form of code bank-switching. The 56800 also implements a conventional software stack, a concession to microprocessor programmers and a boon for compilers.

Other changes not apparent from the programmer's model are the extension of the bit-manipulation unit to 16 bits and a 16-bit barrel shifter. Like the 56100, the 56800 has multiple on-chip data and address buses, and its data memory is dual ported, allowing it to fetch one instruction and make two data references simultaneously.

The company has teamed with software tool-developer Tartan to bring out a suite of C and, in an unusual move for a DSP architecture, C++ programming tools. Like the 56800's internal structure, the availability of a C compiler is intended to make microprocessor programmers feel more at home. Unfortunately, the software is not as far along as Motorola's chips. A beta version of the C compiler isn't due until 2Q96, with the C++ compiler and source-level debugger following by several months.

On the outside, the new 56800 devices even look like microcontrollers. The two initial devices, the 56L811 and 56L812, are nearly identical. Both chips carry a synchronous serial port, a pair of asynchronous serial-peripheral interfaces, three timers, and 32 general-purpose I/O lines. Eight of the I/O pins can interrupt the processor, giving the 56800 chips an unusual amount of interrupt flexibility for a DSP.

Both the '811 and the '812 have 16-bit external address and data buses. They differ only in the type and amount of on-chip memory: the '811 has a 1K program RAM and 2K of data RAM, while the '812 has 22K of program ROM, 2K of data ROM, and 2K of data RAM. Motorola plans more versions near the end of the year, including derivatives with flash memory.

 

## TI Tackles Cost, Adds Flash

Like Motorola, TI created its new low-cost family by leveraging an existing design. In TI's case, the venerable 320C2x core has been updated to create the 320C2xx family. The result is source-code compatible with the 'C2x at the assembler level but offers higher performance, lower prices, and a range of new features.

TI is currently shipping the 320C203 and 'C209 at speeds of 28.6 MIPS. TI has announced plans for no fewer than six initial members of the 320C2xx family with different amounts of memory and peripheral functions; four of the chips will be pin-compatible. For ASIC development, TI is inviting high-volume customers to design around the new DSP core, which it calls the 320C2xLP. Fabricating customer ASICs around a commercial DSP core is an unusual move that could give TI a big leg up in the highest-volume markets.

Table 1 summarizes the differences among the six members of the 320C2xx family. As the table shows, all versions except the 'C209 deliver 40 MIPS peak performance, much faster than their 12.5-MIPS 'C2x predecessors. The first five chips run with a 3.3-V nominal supply, versus the 3.0-V supply used by the two Motorola devices.

## Flash Memory Makes 'F206/207 Stand Out

The 320F206 and 320F207 are almost unique among DSPs in having flash memory on the chip. Even at the highest clock rates, the 32K×16 on-chip flash memory can be accessed with no wait states. The flash is also easy to use—it can be erased and reprogrammed by the CPU under software control or via the chip's JTAG test port. Either way, no special programming voltages are required, just the chip's usual supply. This rare combination of features makes the flash memory ideal for large program stores or for maintaining volatile data.

TI is nearly alone in offering flash memory in a commercial DSP. AT&T's DSP1600 family also offers flash, but at more than $1,000 per device, the AT&T chip is clearly intended only for prototyping.

The flash-based 'F206 and 'F207 are particularly interesting for the role they play in TI's new roadmap for high-volume DSPs. With four pin-compatible versions of the family available, TI customers can start their designs with the RAM-based 'C203 or 'C205, migrate to the ROM-based 'C204 or flash-based 'F206 as volumes increase, and finally end up with a custom ASIC based on the 'C2xLP core. Such a clearly defined series of stepping stones from prototype to high volume should be an important advantage for TI and its customers.

## Prices Designed to Attract New Customers

For both vendors, the prices of these new 16-bit families are as important as the chips' technical features. For example, TI is offering the 'C203 at 28.6 MIPS for only $6.85 in 1,000-unit quantities; Motorola will say only that its new DSPs are priced at "less than $10" in 100,000-piece lots. Both prices set new lows for 16-bit DSPs with respectable performance. Clearly, both companies are gunning for the same high-volume customers, seeking designs in disk drives, consumer electronics, telecommunications equipment, and the like.

Motorola's hardware developments are on roughly the same schedule as TI's, with chips already sampling and production slated to begin at midyear. The company has also put a lot of effort into making the 56800 series appealing to microcontroller and first-time DSP users, an interesting tactic. However, with only two products announced, the 56800 roadmap is not yet clear to us. Although the high-volume customers Motorola is courting will certainly be interested in a clearer roadmap, the current family should satisfy many vendors' immediate needs.

TI's product family seems to be more fully realized, although some members are a bit further off. The 320C2xx family offers a compelling price/performance proposition and a clear and attractive growth path. Both product families are undoubtedly headed for fierce competition in the coming months, promising an interesting range of low-cost, DSP-based consumer items to come. M

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### Price and Availability

Motorola's first 56800-family device, the 56L811, is sampling now. Production is scheduled to begin in 2Q96; pricing will be less than $10 in quantities of 100,000. The 56L812 will begin sampling in 3Q96. For more information, contact Motorola (Austin, Texas) at 800.845.6686; fax 512.891.3877; or via the Motorola DSP Web site at *motserv.indirect.com/dsp/dsphome.html.*

Texas Instruments' 320C203 and 'C209 are currently in production at 28.6 MIPS; availability of the remaining parts is listed in the table below. For more information, contact TI (Denver, Col.) at 800.477.8924 x4500; fax (outside North America) 303.294.3747; or via the Web at *www.ti.com/dsps.*

| | C203 | C204 | C205 | F206 | F207 | C209 |
|---|---|---|---|---|---|---|
| Speed (MIPS) | 40 | 40 | 40 | 40 | 40 | 28.6 |
| RAM (words) | 544 | 544 | 4.5K | 4.5K | 4.5K | 4.5K |
| ROM (words) | None | 4K | None | None | None | 4K |
| Flash (words) | None | None | None | 32K | 32K | None |
| Sync Serial | 1 | 1 | 1 | 1 | 2 | None |
| Async Serial | 1 | 1 | 1 | 1 | 1 | None |
| Package | TQFP | TQFP | TQFP | TQFP | TQFP | TQFP |
| Pins | 100 | 100 | 100 | 100 | 144 | 80 |
| Samples | 2Q96 | 2Q96 | 3Q96 | 2Q96 | 4Q96 | Now |
| Production | 3Q96 | 3Q96 | 4Q96 | 4Q96 | 1Q97 | Now |

**Table 1.** The six initial members of TI's 320C2xx family are nearly identical, and four members are pin-compatible. The chips differ mainly in the type and amount of on-chip memory they contain.

 