Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. Patents related to microprocessors issued recently. Please e-mail comments or criticisms to belgard@umunhum.stanford.edu.

5,438,668
System and method for extraction, alignment and decoding of CISC instructions into a nano-instruction bucket for execution by a RISC computer
Issued: August 1, 1995
Inventors: Brett Coon, et al
Assignee: Seiko Epson
Filed: March 31, 1992
Claims: 29
A system and method for extracting complex, variable-length computer instructions from a stream of instructions, each subdivided into variable numbers of bytes, and aligning instruction bytes of individual complex instructions. The system receives a portion of the stream of complex instructions and extracts a set of instruction bytes starting with the first instruction bytes, using an extract shifter. This set of instruction bytes is then passed to an align latch where the bytes are aligned and output to a next-instruction detector. The next-instruction detector determines the end of the first instruction based on said set of instruction bytes. An extract shifter is used to extract and provide the next set of instruction bytes to an align shifter which aligns and outputs the next instruction. The process is then repeated for the remaining instruction bytes in the stream of complex instructions. The isolated complex instructions are decoded into nano-instructions, which are processed by a RISC processor core.

5,438,646
Feed-forward neural network
Issued: August 1, 1995
Inventor: David Davidian
Assignee: NEC
Filed: August 19, 1992
Claims: 4
A forward-feed neural network is disclosed using data-flow techniques based on a data-flow microprocessor. This implementation is simpler and faster because of an inherent similarity between the flow of information in the brain and in a data-flow architecture.

5,437,039
Servicing transparent system interrupts and reducing interrupt latency
Issued: July 25, 1995
Inventor: Desmond Yuen
Assignee: Intel
Filed: April 13, 1993
Claims: 15
A system management interrupt (SMI) handler comprising a plurality of service tasks is provided for a computer system to service SMIs. The service task execution is interleaved with normal execution. An SMI task queue stores incidences of the service tasks for servicing SMIs. An SMI trigger mechanism, comprising a timer, is reserved for triggering execution of the service tasks. A register is predesignated to store an SMI status word for differentiating an SMI is triggered by the reserved SMI trigger mechanism from other SMIs triggered by other general-purpose SMI trigger mechanisms. As a result, the interrupt latency for servicing an SMI is reduced.

5,434,987
Method and apparatus for preventing incorrect fetching of an instruction of a self-modifying code sequence with dependency on a buffered store
Issued: July 18, 1995
Inventors: Jeffrey Abramson, et al
Assignee: Intel
Filed: December 5, 1994
Claims: 24
A number of identical matching circuits are integrated into the store address buffer, one to each buffer slot, for comparing the address of an instruction being fetched and the corresponding portions of the store destination addresses of the buffered store instructions. A stall signal generator is provided for generating a single stall signal to the bus controller, using match signals, thereby stalling an instruction fetch from a source address that is potentially a store destination of one of the buffered store instructions.

Other Issued Patents
5,438,669 *Data processor with improved loop handling utilizing improved register allocation*
5,437,016 *Apparatus and method for translating logical addresses for virtual machines*
5,434,989 *Cache memory for efficient access with address selectors* ♦

