Most Significant Bits

TI, SGS Add 486DX4 to Lineup

Both Texas Instruments and SGS-Thomson are now shipping 100-MHz 486DX4 parts. These chips, based on Cyrix's 486 design, are clock-tripled 486s with an 8K write-back cache. TI has priced its chip at $70, while SGS sells its DX4 for $60, both in quantities of 1,000. The SGS part is available today; TI is sampling its DX4 and plans volume production in January.

To achieve the higher clock speed, both companies have moved to more advanced IC processes, TI using a 0.42-micron process and SGS going to 0.35 microns. As a result, the parts have slightly lower power consumption than other DX4s, including AMD's and Intel's: at 100 MHz, the new parts consume 2.1 W (typical).

SGS added a new 486 pinout, moving the write-back cache signals for compatibility with Intel's DX4; the parts are also available in the old Cyrix-compatible pinout.TI offers only the Cyrix pinout, although it is considering an Intel pinout in the future. This is the final Cyrix design that TI will receive; the company is developing its own Pentium-class core to extend its x86 line. SGS has the right to sell 5x86 and 6x86 parts but has not exercised that option, although it probably will soon.

Cyrix, IBM Announce New 5x86s

Expanding its product line, Cyrix has introduced a 120-MHz version of its 5x86 processor *(see **090901.PDF**)*. The company rates the new chip at the same performance level as a Pentium-90. On Winstone 95, the 5x86-120, using a Diamond Stealth graphics card, scores 10% better than a Dell P90 system with a Number Nine card, but the Cyrix chip fares 15% worse on CPUmark16, a benchmark more focused than Winstone on CPU performance. At $160, the chip, which uses a 486 pinout, is priced the same as a 75-MHz Pentium. Cyrix also trimmed the list price of the 100-MHz 5x86 to $130.

The new version uses the same die as the original 5x86. The 0.65-micron process is now yielding well at the higher clock speed, enabling the new product. The 120-MHz version is sampling now, with volume production expected later this month. At Comdex, Cyrix plans to demonstrate a 120-MHz 6x86, a part that should be formally introduced by the end of the year.

IBM recently announced its version of the 5x86, called the 5x86C but otherwise identical to Cyrix's part. Unlike Cyrix, IBM is offering a 75-MHz speed grade as well as a 100-MHz version. The full-speed part carries a 1,000-piece list price of $131, almost matching Cyrix's price. The 75-MHz 5x86C, which offers about the same performance as a 100-MHz DX4 and uses the same pinout, goes for $109. This seems high compared with pricing for the DX4 parts from TI and SGS-Thomson.

Intel Bombs Price of Fast Pentiums

Making room for Pentium Pro *(see **091501.PDF**)* as well as for pending high-speed Pentiums, Intel again slashed the price of its Pentium product line. Sandwiched by the frighteningly customary 25%-per-quarter drops for the 100- and 133-MHz parts, the price of the Pentium-120 dove nearly 40% to $357, slotting that chip at a price 20% higher than that of the Pentium-100. Intel says that its 0.35-micron capacity is ramping more quickly than anticipated, allowing the price of the 120-MHz part to fall. The table below compares the new 1,000-piece list prices, effective now through the end of January, with current list prices from Intel's competitors.

		3Q95*	4Q95*	%CHG
Intel	Pentium-133	$694	$520	–25%
	Pentium-120	$581	$357	–39%
	Pentium-100	$398	$300	–25%
	Pentium-90 VRT	$341	$272	–20%
	Pentium-90	$291	$247	–15%
	Pentium-75 VRT	$204	$178	–13%
	Pentium-75	$184	$158	–14%
Cyrix	6x86-100	—	$450	—
	5x86-120	—	$160	—
	5x86-100	$147	$130	–12%
AMD	Am5x86-133	—	$93	—
	486DX4-120	$165	$83	–50%
	486DX4-100	$122	$75	–39%
TI	486DX4-100	$110	$70	–36%
	486DX2-80	$80	$40	–50%
	486DX2-66	$66	$40	–40%

*Intel 3Q prices effective 7/31; Intel 4Q prices effective 11/1

Intel's high-end prices are falling to make room for 150-MHz and 167-MHz parts due in the next few months. Prices for Intel's low-end Pentiums eased more slowly, about 15% for the 75- and 90-MHz parts. The Pentium-75 has now reached $158.

As the market moves to Pentium, 486 demand is falling even as several suppliers are gearing up production. This supply/demand imbalance caused 486 prices to fall 40–50% last quarter, dropping the price of a DX2 below $50 and that of a DX4 well below $100.

AMD Turns 486 into Am5x86...

Unable to move to a true Pentium-class core, AMD has responded to falling 486 prices by introducing a 133-MHz 486DX4 as the Am5x86-P75. The suffix indicates AMD's assertion that the chip delivers integer performance similar to a 75-MHz Pentium's. On floating-point applications, the Am5x86 will fare much worse.Thus, the name is doubly misleading, as the chip doesn't delivers full Pentium performance and is not a version of the Cyrix 5x86; it's just a 486DX4 in 586 clothing.

The device, previously known as the X5, is a 0.35-micron version of the company's 486 core combined with a 16K write-back cache. Its 486 pinout is compatible with that of Intel's write-back 486 parts. The new die is a tiny 43 mm^2 despite the doubled cache size. The MDR Cost Model estimates that the chip costs about $25 to manufacture, slightly less than AMD's 0.5-micron 486 and 20% less than Intel's DX4. The new chip is now in production at AMD's Sunnyvale (Calif.) fab as well as its new Fab 25, representing the first production product from the latter facility.

The rapid collapse of 486 prices is forcing AMD to sell the Am5x86 for less than $100. Apparently, the company doesn't believe that PC makers will accept this part as a Pentium-75 equivalent, and thus it will offer the chip at $93 in quantities of 1,000, a 40% discount from the Pentium's price. We believe AMD will find it difficult to significantly exceed the $100 price range until it launches the K5 in the middle of next year.

...and Positions 486 for Embedded

AMD's new 486DE2-66 is essentially identical to its 486DX2-66 processor, providing an 8K write-back cache, an FPU, and a 33-MHz 32-bit bus interface. The only differences between the 486DE2 and the DX2 are the embedded chip's optional 1× clocking mode and SQFP-208 package. The 3.3-V chip is now in production using a 0.5-micron CMOS process; a 0.35-micron version with an enlarged 16K cache (similar to the Am5x86) will follow early next year.

The key to AMD's embedded initiative is its commitment to freeze the definition of the 486DE and keep it in production for several years. Embedded designers had been hesitant to commit to the 486DX2 because of constant minor changes and concern that AMD would drop the product after the K5 debuts.

Although AMD is the third company to announce an embedded 486, its chip is the first to reach production. National's 486SXF *(see **091201.PDF**)* is expected later this quarter, but Intel's Hummingbird chips *(see **091303.PDF**)* aren't due until 2Q96. At $56 in 10,000-piece quantities, AMD's offering is priced below Intel's, but National's chips are much less expensive, just $15 to $25. Unlike AMD or Intel, National has included on-chip peripherals, but its chips cannot run DOS or Windows.

At 66 MHz, the 486DE runs at twice the speed of other embedded 486s. Its write-back cache gives the AMD chip an additional performance edge in systems without an external cache, which are the majority of embedded designs. National's 486 chips are cheaper, and Intel's consume less power, but AMD offers the only choice for customers who want a chip with high performance (particularly on floating-point code), DOS compatibility, and modest cost.

Opti Adopts UMA for Viper Chip Set

Opti's Viper-UMA (unified memory architecture) chip set is the first Pentium core-logic product to adopt the emerging VESA UMA standard. It consists of three chips: a system controller (82C567), a 64-bit datapath chip (82C566), and a peripheral controller (82C568). The system controller controls the DRAM, L2 cache, and PCI. The peripheral controller bridges PCI and ISA, supports IDE, and manages system power. The datapath chip buffers the CPU, PCI, and DRAM.

Viper-UMA improves performance by giving graphics and video peripherals direct access to the 64-bit-wide main-memory bus instead of the narrower PCI bus. It reduces cost by combining the graphics frame buffer with main memory. To ease contention between graphics and CPU accesses, Viper-UMA implements extensive buffering between the CPU and DRAM, the CPU and PCI, and the system controller and PCI. To reduce refresh bandwidth, graphics vendors should incorporate data compression schemes like those used in Cyrix's 5gx86 processor and Weitek's UMA chip set.

Unlike Weitek, Opti relies on graphics vendors to provide the UMA graphics controller. So far, Trident's TGUI9682 64-bit graphics controller is the only chip that supports Opti's Viper-UMA. S3 says its future graphics controllers will be compatible with Opti-like approaches. The Opti chip set will also work with conventional graphics controllers using a non-UMA design.

Opti is working through the Video Electronics Standards Association (VESA) to standardize its approach. Opti chairs the sub committee that is defining VESA's version of UMA: VUMA. Companies such as ATI, Cirrus Logic, S3, and Trident have been instrumental in the development of VUMA, which will soon be introduced as a VESA standard. To work together under VUMA, both the graphics and memory controllers must implement a simple arbitration protocol.

Previous Viper chip sets have been criticized for a lack of PCI performance. Opti's designers fixed this problem in the latest product by eliminating VL-bus support and optimizing the chip for PCI, boosting PCI bandwidth beyond 100 Mbytes/s. Another improvement is the addition of enhanced IDE bus mastering. The Viper-UMA is sampling now with volume production by February. Like previous Viper versions, the new chip set is priced at $25 in quantities of 10,000.

We expect many PC makers to build UMA systems in the coming year. Because Intel is not expected to deliver a UMA chip set until 2H96, the Opti product should be popular in the interim, allowing system vendors to reach lower price points than PCs that use Intel motherboards.

LSI Repacks High-End MIPS Core

At last month's Microprocessor Forum, LSI Logic re-

vealed that it has redesigned its high-end CW4010 MIPS processor core, moving it to a smaller, lower-voltage manufacturing process. The new CW4020 core runs at up to 133 MHz and is promised to deliver well in excess of 120 Dhrystone MIPS. The 0.35-micron core will be available for production use by mid-1996, at which time the 0.5-micron 4010 will be obsoleted.

The internal organization of the 4020 core maintains the five-stage, two-issue pipeline structure of its predecessor. The core fetches and decodes two instructions simultaneously, dispatching them to as many as five execution units. Based on simulated C code, LSI estimates the 4020 executes an average of 1.3 instructions per clock cycle; optimized assembly code may do up to 20% better.

The 4020 was hand-optimized for LSI's 0.35-micron three-layer-metal CMOS process. At its top speed of 133 MHz, the static core dissipates 1.3 W, or 10 mW/MHz. An intermediate version, the CW4011, is an optical shrink of the 4010 to the same 0.35-micron process; it measures 9.5 mm^2 (without caches). LSI did not reveal the die size of the new core but said that the redesign did not achieve significant area savings.

The smaller geometry boosts the clock speed but forced LSI to reduce the supply voltage to 2.5 V from the 4010's 3.3 V. New ASIC customers aren't likely to complain too loudly; 2.5-V cores are becoming more common as power consumption becomes a critical issue in emerging high-performance consumer applications.

The new LSI core is one of the most powerful yet announced, but its performance is dwarfed by that of Digital's StrongArm *(see **091504.PDF**)*, which delivers as much as 240 Dhrystone MIPS. StrongArm also consumes less power and, at 4.3 mm^2, is much smaller than the 4020. LSI has much more experience in the ASIC business and a broad range of peripherals to choose from, giving it an edge over Digital unless an application requires the extreme performance of StrongArm.

C-Cube Acquires MicroSparc License

Showing the first fruits of a renewed push into the 32-bit embedded market, SPARC Technology Business (STB) has signed C-Cube Microsystems as its latest MicroSparc licensee. C-Cube, which recently hired former SPARC architect Les Cohn, will use the MicroSparc-1 core in a new line of multimedia accelerator chips, beginning with a combination MPEG-2/videoconferencing controller. The chip will perform MPEG-2 compression and decompression and support the H.320 and H.324 videoconferencing standards.

C-Cube had previously relied on its own proprietary VideoRisc core design for intelligent MPEG chips, but the company chose the MicroSparc-1 core for future designs to reduce its investment in proprietary hardware and software development tools. With a standard SPARC core, C-Cube's customers will be able to use existing third-party SPARC tools. The company will continue to expand its line of VideoRisc chips but intends to use MicroSparc for its higher-end products.

The financial terms of the agreement between the companies were not disclosed, but C-Cube gains rights to the MicroSparc-1 core only, not to MicroSparc-2 or to UltraSparc's VIS (visual instruction set) multimedia extensions. The terms of the agreement permit C-Cube to modify the core or instruction set with its own proprietary extensions, but the company has not announced any plans to do so.

Hyundai already uses a MicroSparc-1 core as the heart of its MPEG-2 chip *(see **0905MSB.PDF**)*. The French vendor Matra MHS is also developing SPARC-based microcontrollers, and Xerox recently announced Document Center products based on embedded SPARC chips. After a quick start in the embedded market, SPARC has languished in recent years, losing ground to more aggressive vendors. Now, with new licensees and an optimistic roadmap that promises a new embedded SPARC core roughly every 12 months, STB is moving to improve its position in the embedded processor race.

Errata: Supercomputers

In a recent editorial *(see **0913ED.PDF**)*, we incorrectly characterized the maximum number of processors in several high-end RISC systems. According to their vendors, the Cray T3D supports up to 2,048 processors; IBM's SP2 allows up to 512 CPUs in some configurations; and SGI's Challenge boxes hold up to 36 processors. ♦

