UltraSparc to Pick Up Speed in 1996

By End of 1996, UltraSparc-2 to Hit 300 MHz while Halving Die Size

by Linley Gwennap

Even as it rolls out the first UltraSparc systems (see sidebar), Sun revealed its plans to deliver faster versions of that processor. Taking advantage of Texas Instruments' improving IC manufacturing capabilities, Sun expects to deliver 200-MHz UltraSparc-1+ parts in 2Q96, followed in 3Q96 by UltraSparc-2 chips that run at 250 to 300 MHz. Figure 1 shows the new roadmap.

Increasing the clock rate on its high-end design should help Sun catch up with the integer performance of Intel's Pentium Pro (see cover story) and surpass next-generation PowerPC, MIPS, and PA-RISC chips. Another advantage of the forthcoming die shrinks is a reduction in cost.

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At the Forum, Anant Agrawal, Sun's VP of CPU development, maps the future of UltraSparc.

Quick Shrink Boosts Clock

The initial UltraSparc design (US-1) is built in a 0.47-micron four-layer-metal CMOS process. This die measures 315 mm^2 and is now in production at speeds up to 167 MHz, with parts sampling at 182 MHz. Sun has done an excellent job of meeting and even exceeding the clock-speed goal set at the initial introduction *(see **081301.PDF**)*. At 182 MHz, the chip exceeds the original performance goals for both integer and floating point, although the integer performance is a bit behind on a clock-for-clock basis. System shipments for the chip are about a quarter behind schedule, not unusual for such a complex device.

To move beyond 182 MHz, Sun will move the original design to TI's 0.42-micron process, a 10% optical shrink. The smaller transistors will allow speeds of 200 MHz and possibly beyond. This version cuts the die area to 265 mm^2. The company is already sampling this chip, dubbed UltraSparc-1+ (US-1+), and demonstrated a 212-MHz version at last month's Microprocessor Forum. Sun expects to deliver 200-MHz parts in 2Q96 but has not committed to speeds beyond that from US-1+.

UltraSparc-2 Takes Big Step

The original UltraSparc was designed for TI's mature EPIC-3 process to reduce risk, said Sun's Anant Agrawal at last month's Microprocessor Forum. With that design now verified and in production, the two companies are working to move the design into the leading-edge EPIC-4 process, yielding benefits in cost, clock speed, and power consumption.

EPIC-4 *(see **090905.PDF**)* is a 0.29-micron CMOS process that surpasses any microprocessor process in production today in both speed and density. By the time EPIC-4 reaches production, 0.3-micron processes from Intel and IBM will challenge EPIC-4 on speed. TI's ability to deliver tight metal pitches (1.2 microns) for metal 1 through metal 4 and add a fifth global routing layer should make EPIC-4 the densest process available for high-transistor-count microprocessors.

UltraSparc-2 (US-2) takes advantage of this density to achieve a 149-mm^2 die size, less than half the size of the US-1 design. Although EPIC-4 carries a higher wafer cost than its predecessor, US-2 should have a manufacturing cost of about $160, about half the cost of US-1. This cost will decline to about $120 as the new process matures, according to the MDR Cost Model, making US-2 only 50% more costly to build than Pentium and much cheaper than even a 0.35-micron Pentium Pro.

The smaller transistors and die size will improve the clock speed to 300 MHz, according to Agrawal. This should boost performance as high as 11 SPECint95 and 18 SPECfp95 (baseline) at 300 MHz. As an added benefit, changing the power supply from 3.3 V to 2.5 V reduces power consumption to 24 W (at 300 MHz), despite the jump in clock frequency.

New Features in UltraSparc-2

While US-2 is largely identical to its predecessor from a functional standpoint, Sun took the opportunity to add a few new features. The new design allows the cache SRAMs to run at two-thirds of the CPU clock speed, for example, 5 ns at 300 MHz. This mode halves the available cache bandwidth, but latency is extended by only one cycle. With a full-speed cache, sending the address, accessing the SRAM, and receiving the data take one cycle each; with the slower cache, the address is sent in the first two cycles, and the data is read in the next two cycles—a total of four cycles.

The new design also adds prefetch instructions, sim-

Price & Availability

UltraSparc is available from Sun's SPARC Technology Business (STB). The company is shipping 143-MHz and 167-MHz parts in volume and sampling 182-MHz and 200-MHz parts. Sun expects the latter two parts to achieve volume production in 1Q96 and 2Q96, respectively. UltraSparc-2 is not formally announced.

In quantities of 1,000, the 143-MHz part sells for $995, while the 167-MHz part sells for $1,395. The 182-MHz version will list for $1,595. No pricing is set for the 200-MHz chip. For more information, contact STB at 408.774.8545 or access the Web at *www.sun.com/stb*.

First UltraSparc Systems

The first systems using the UltraSparc processor are a series of workstations from Sun creatively dubbed the Ultra 1 family. Realizing the weakness of using SuperSparc in the midrange, Sun is offering very aggressive pricing on the Ultra 1, starting at just $16,495. At this price, the entry-level Model 140 comes with a 143-MHz UltraSparc, 512K of cache, 32M of memory, a 1G disk, and a 17" color monitor. This system is rated at 215 SPECint92 and 302 SPECfp92 (peak).

Most other Ultra 1 systems feature 167-MHz CPUs. The least expensive of these is the Model 170, which costs $22,995 but is robustly configured with 512K of cache, 64M of memory, a 2G disk, and a 20" color monitor. This unit delivers 252 SPECint92 and 351 SPECfp92 (peak). None of the systems use faster versions of UltraSparc; all are available by the end of November.

The performance of these systems appears to exceed that of any other shipping workstation except for Digital's high-end Alpha units. Hal Computer had recently grabbed the title of the fastest SPARC workstation *(see **0913MSB.PDF**)*, but even the entry-level Model 140 delivers better performance than Hal's best system, and does it at half the price.

Unfortunately, Sun chose not to release SPEC95 ratings for its new systems, making an accurate performance comparison difficult. The company promises to divulge these numbers soon. In the meantime, Figure 1 shows our conservative estimates.

ilar to those in other architectures, that allow the compiler to hide memory latency by requesting instructions and data before they are needed. Finally, the bus interface is modified to support multiple outstanding requests per processor: up to three loads (cache misses) and two stores (writebacks). The UltraSparc system bus *(see **090703.PDF**)* is designed to handle multiple transactions, but US-1 chips process only one transaction at a time.

The latter two changes work hand in hand to improve performance. By overlapping transactions, US-2 can execute prefetch instructions without delaying normal memory traffic. On the DAXPY (matrix multiply) inner loop, for example, overlapped transactions alone provide no benefit, and prefetching alone increases performance by 57%. Combining both features, however, boosts performance by 107%. These improvements are particularly important for commercial applications (e.g., on-line transaction processing) and for scientific code with large data sets, including some SPECfp95 tests.

Improving SPARC's Competitiveness

Sun expects US-2 to tape out by year-end and ship in systems in 3Q96. This relatively short schedule is achievable for a part with few functional changes. If all goes well, UltraSparc clock speeds should nearly double within a year of first shipments. Integer performance will increase at about this pace, but the changes in US-2 will improve SPECfp95 scores by even more than the clock-rate increase, putting that part on par with the FP performance leaders.

If Sun delivers on this plan, US-2 will exceed the performance of all other processors expected to ship in 1996, except for Digital's 21164A. Shrink versions of the Pentium Pro, PA-8000, and R10000 should also surpass US-2, at least in integer performance, but these versions are not due until 1H97. US-2 will have an edge on its competitors in processor manufacturing cost and, particularly versus the PA-8000 and 21164, in system cost.

The functional changes in US-2 focus it on two markets, servers and scientific computation, where it has clear advantages over Pentium Pro. For servers, UltraSparc offers greater memory bandwidth than any other microprocessor. The new features allow US-2's SPECfp95 rating to challenge those of its top RISC rivals and improve OLTP performance as well. The VIS multimedia extensions *(see **081604.PDF**)* give the chip another edge. UltraSparc, and particularly US-2, will help Sun deliver better price/performance than other RISC system vendors while positioning it in market niches that can withstand the onslaught of Pentium Pro. ♦

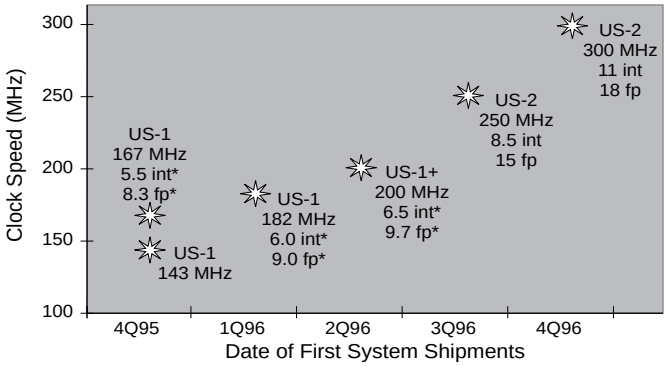

Figure 1. Sun's plans include faster versions of UltraSparc every quarter throughout 1996. The figure provides SPEC95 (baseline) performance for each chip. (Source: Sun except *MDR estimates)

