Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

5,428,779
System and method for supporting context switching within a multiprocessor system having functional blocks that generate state programs with coded register load instructions
Issued: June 27, 1995
Inventors: Jean D. Allegrucci, et al
Assignee: Seiko Epson
Filed: November 9, 1992
Claims: 4
A context switching system for saving, restoring, or swapping tasks is adapted for use in a multitasking processor coupled to an external or system memory. The processor includes one or more functional blocks. The functional blocks comprise registers representing the context of the system. The system comprises a controller that receives a save or switch command and generates a context-save instruction. The controller is configured to pass the context-save instruction to the functional blocks. The functional blocks generate a state program. The state program consists of register-load instructions and the state data representing the context of the system, so that context can be restored at a later time. The state program is stored in an external or system memory.

5,426,766
Microprocessor which holds selected data for continuous operation
Issued: June 20, 1995
Inventor: Koji Ogata
Assignee: NEC
Filed: August 23, 1994
Claims: 3
A microprocessor includes a switching register bank having switching registers corresponding to the respective data registers of data register banks. Updating each output register of a bank is determined on the basis of the stored contents of a corresponding switching register of the switching register bank. Since part of the stored contents of the output register bank can be continuously used without a copy operation, the processing speed can be increased.

5,426,743
Three-to-one arithmetic logic unit for simultaneous execution of an independent or dependent add/logic instruction pair
Issued: June 20, 1995
Inventors: James E. Phillips, et al
Assignee: IBM
Filed: January 24, 1994
Claims: 8
A high-speed three-to-one data-dependency-collapsing ALU can be used to support multiple issue of instructions. As the computing apparatus supports multiple issue of instructions, it is useful in CISC, superscalar, superscalar RISC, etc computer designs. The apparatus allows the execution of any combination of two independent or dependent arithmetic or logical instructions in a single machine cycle.

5,423,047
Methods and apparatus for using address-transition detection to reduce power consumption
Issued: June 6, 1995
Inventor: David A. Leak
Assignee: Intel
Filed: June 22, 1993
Claims: 14
A method and apparatus for using address-transition detection in a device to reduce power consumption. A circuit for address-transition detection and power reduction for the device detects address transitions on an address bus. The address-transition-detection circuit enables circuits for processing the new data for the new address transition. Thereafter, the device processes the new address. The address-transition circuit then disables the circuits for processing the address transition to reduce DC power consumption until the next address transition is detected.

Other Issued Patents

5,428,748 *Method and apparatus for automatically configuring a computer peripheral*
5,428,746 *Integrated microprocessor unit generating separate memory and input/output device control signals*
5,426,742 *Microprocessor for supplying branch condition indicating signal in response to execution of conditional branch instruction*
5,426,744 *Single-chip microprocessor for satisfying requirement specification of users* ♦

