Six DRAM Vendors Back 64M Rambus Chip

New Part, to Debut in 1997, Aimed at Main-Memory Applications

by Linley Gwennap

Continuing to gain momentum, Rambus has rolled out its plans for a 64-Mbit RDRAM with backing from six DRAM vendors, including the largest four in the world. Samsung, Hitachi, NEC, Toshiba, LG Semicon (formerly Goldstar), and Oki all plan to produce the new part, which is not expected to reach production until 1997. Rambus has already established its RDRAM as one of the leading alternative DRAM architectures and hopes that its new part will allow it to move beyond the graphics frame buffer into PC main-memory applications.

The six backers together hold nearly half of the current DRAM market share. Hitachi is a newcomer to the team and will start producing RDRAMs at the 64M level; the others are currently building 16M Rambus chips. Production of these parts is beginning to ramp, with volumes reaching the tens of thousands per month.

64M Part Offers Improvements

In the 64M generation, the overhead of the Rambus interface becomes a smaller part of the die (less than 5%). In fact, at this level the RDRAM has about the same die size as a 32-bit-wide EDO DRAM, which Rambus expects to be the volume DRAM part in 1997. The vendors plan to charge only a small price premium for RDRAM compared with EDO DRAM. Even today, a 16M RDRAM sells for about the same price as four 256K×16 parts while offering much better bandwidth.

In addition to larger capacity, the 64M version contains a few improvements over the current parts *(see **070304.PDF**)*. The clock speed of the Rambus has been increased slightly from 250 to 266 MHz, conveniently four times the 66-MHz bus speed used in many PCs. By delivering data on both clock edges, the 8-bit Rambus can achieve a 533-Mbyte/s bandwidth. This peak bandwidth exactly matches that of the Pentium and Pentium Pro (P6) system buses.

The 64M part has four internal banks, twice as many as the 16M RDRAM, to reduce bank conflicts and increase concurrency. The chip can overlap two requests as long as they are to different banks. Rambus also redesigned the interface to reduce latency, bringing it more in line with EDO and other competitive solutions.

Main Memory for Next-Generation CPUs

RDRAM has recently gained momentum as a frame buffer solution, with design wins at Cirrus Logic, Nintendo, and Silicon Graphics *(see **0910MSB.PDF**)*. The 64M part is aimed squarely at PC main memory. Three trends favor RDRAM: unified memory architecture (UMA), concurrent buses, and granularity.

The unified memory architecture *(see **090801.PDF**)* combines the frame buffer and main memory. We expect this design to become popular in 1996 as a way of reducing system cost. UMA, however, puts greater bandwidth demands on the combined memory subsystem, which can cause performance degradation in systems with standard DRAM. The higher RDRAM bandwidth reduces performance loss.

The concurrent bus of the Pentium Pro is unique among x86 processors in pipelining several transactions at once. A single 64M RDRAM can handle two concurrent transactions while supplying data at the full burst rate of the Pentium Pro bus. Intel expects initial Pentium Pro systems to use a four-way interleaved DRAM system to accomplish the same task, pushing the minimum main-memory size to 64 Mbytes with 2M×32 chips, versus 8 Mbytes for the 64M RDRAM design.

Although the interleaved solution is fine for servers, the smaller granularity of the RDRAM design is better for low-cost desktops, which won't be able to afford 64 Mbytes of memory any time soon. In 1997, Pentium Pro should be entering the mainstream desktop market, just as the 64M RDRAM is scheduled to begin production.

Competitors Lag in Support

Even Rambus backers admit that EDO DRAM will be the volume memory for the next couple of years, taking over from fast-page-mode DRAM. But there is a growing opportunity for a truly alternative DRAM architecture that solves the performance and granularity problems noted above. The RDRAM's strongest competition should come from synchronous DRAM *(see **070205.PDF**)*, but even that JEDEC-standard design has yet to see many design wins. If the RDRAM vendors can deliver on their cost promises, the 64M part will be well positioned to take a chunk of the PC main-memory market later this decade. ♦

For More Information

The 64M Rambus DRAM will not be available in volume production until 1997. For more information, contact Rambus (Mt. View, Calif.) at 415.903.3800; fax 415.965.1528.

