Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

5,423,014
Instruction fetch unit with early instruction fetch mechanism
Issued: June 6, 1995
Inventor: Glenn J. Hinton
Assignee: Intel
Filed: February 24, 1994
Claims: 5
An instruction fetch unit in which an early instruction fetch is initiated to access main memory simultaneously with checking a cache for the desired instruction. On a slow path to main memory is a large main translation lookaside buffer (TLB) that holds address translations. On a fast path is a smaller translation write buffer (TWB), a mini-TLB that holds recently used address translations. A guess fetch access is initiated by presenting an address to the main memory in parallel with presenting the address to the cache. The address is compared with the contents of the TWB for a hit and with the contents of the cache for a hit. The guess access is allowed to proceed upon the condition that there is a hit in the TWB (the TWB is able to translate the logical address into a physical address) and a miss in the I-cache. The guess access is canceled upon the condition that there is either a miss in the TWB (the TWB is unable to translate the logical address into a physical address) or a hit in the I-cache. In this case, a fetch access is reissued on the "slow" path that goes through the large main TLB.

5,422,523
Apparatus for translating logic signal levels from 3.3 volts to 5 volts
Issued: June 6, 1995
Inventor: Meeling Roberts
Assignee: Intel
Filed: September 22, 1993
Claims: 13
An apparatus having a 3.3-V power supply and a 5-V power supply wherein digital signals processed on a 3.3-V basis are translated to a 5-V basis by a voltage-translation circuit before being output. The voltage translator is comprised of an inverter for inverting an input signal. The inverter is powered by the 3.3-V power supply. A p-channel transistor having its source coupled to the 5-V power supply and its gate driven by the output of the inverter is implemented. When the inverter generates a low logic level, the p-channel transistor is turned on and outputs 5 V. An n-channel transistor having its source coupled to ground and its gate driven by the output of the inverter is also implemented. When the output of the inverter is 3.3 V, the n-channel transistor is turned on, which pulls the output to ground. Therefore, when the input signal is at 3.3 V, a 5-V signal is output from the voltage-translation circuit. When the input signal is at 0 V, the output signal is likewise at 0 V.

5,421,026
Data processor for processing instruction after conditional branch instruction at high speed
Issued: May 30, 1995
Inventors: Yoshikuni Sato, et al
Assignee: NEC
Filed: March 31, 1994
Claims: 5
A data processor includes a first circuit for decoding a sequence of instructions, including a conditional branch instruction, in such a manner that the conditional branch is decoded and a subsequent instruction is fetched before a branch condition for the branch instruction has settled. The first circuit generates an operand address for the decoded instruction and a first signal indicating that the operand address is the one generated before a branch condition is decided. A second circuit generates, after the decision of the branch condition, a second signal indicating whether or not an instruction decoded after the conditional branch instruction is executed. A control circuit receives the first and second signals and operates to hold off replacement of a portion of the associative memory.

5,421,022
Apparatus and method for speculatively executing instructions in a computer system
Issued: May 30, 1995
Inventors: Francis X. McKeen, et al
Assignee: Digital
Filed: June. 17, 1993
Claims: 21
A compiler groups instructions into sets. The sets of instructions are related by data and control dependencies that are unresolvable by the compiler. Sets of instructions having unresolved dependencies are executed in a speculative state of the computer system under the assumption that an exception condition will not occur. However, if an exception condition does occur during execution of a set of instructions in the speculative state, that exception is detected and the set of instructions is re-executed in a real state of the computer system to resolve the exception condition. ♦

