SGS-Thomson Debuts New 32-Bit Micro

ST20450 Has New CPU Core, Impressive Code Density

by James L. Turley

Just when it seemed that every conceivable microprocessor architecture and instruction set had already been invented, SGS-Thomson has developed a new instruction set and announced the first CPU core to include it. The new core, called the ST20, is touted as a RISC processor, although it uses variable-length instructions that it executes in varying amounts of time. What is clear is that the new microprocessor boasts impressive code density, making it attractive to cost-conscious designers of telecommunications, navigation, and network-infrastructure equipment.

The ST20450 is the first part to be announced that uses the ST20 core. The European semiconductor giant is also nearing completion of several customer-specific designs, which it will announce in the coming months. This article describes the ST20450 microprocessor; in a later issue, we will provide a more in-depth analysis of the chip's underlying architecture and instruction set.

New Architecture, Instruction Set Premiere

The ST20 core was developed from the ground up at SGS-Thomson. It is a new design, which the company oxymoronically calls a "true variable-length RISC." There are three variants of the core, all based around similar 32-bit register files and compact instruction sets.

The C1 version, the smallest core of the lot, has a single execution unit and runs at 0–33 MHz. The C2 core adds a hardware microkernel, or scheduler, and boosts the top speed to 50 MHz. The C4 core, on which the ST20450 is based, has all the features of the C2 plus an independent arithmetic acceleration unit with a three-cycle 32×32 integer multiplier.

The chip includes 16K of SRAM in lieu of a cache, which the processor can access in two clock cycles, a pair of timers, a memory controller, four serial communications channels, and an interrupt controller.

Instructions can be 8, 16, or 32 bits in length, with commonly used instructions encoded in a single byte. Execution time for the majority of instructions varies between one and three clock cycles, with a few instructions lingering in the pipeline for seven cycles or more.

The company evaluated several hundred thousand lines of compiled application code and claims the resulting average instruction length is just 10 bits, implying that the great majority of instructions are of the 8-bit kind, with some 16-bit and 32-bit instructions mixed in. This is a surprisingly compact size, and far better than a "true" 32-bit RISC chip. That instruction size places the 20450 ahead of the 68000 family and Hitachi's SuperH chips, both of which have a minimum instruction length of 16 bits. The '450 is closer to an 8086 or Z80 in terms of assembled instructions per byte of memory. What is not known is the number of instructions required for a given task, the vital second ingredient needed to evaluate code density.

Its core performance should be on par with that of other 32-bit microprocessors. Using the same compiled instruction mix, the average execution time is 1.25 clocks/instruction. This average reflects the part's unequal execution time for common instructions and assumes zero-latency memory. At 50 MHz, then, the part can average 40 native MIPS. Dhrystone numbers are not available, so it is unclear how much useful work those 40 million instructions can accomplish.

Programs executing from the on-chip SRAM should achieve this speed, as the CPU requires about one byte per cycle while the SRAM delivers four bytes every two cycles. External memory may not be so fast.

Serial Links Lifted from Transputer

The ST20450, shown in Figure 1, has lifted one of its most unusual features, its synchronous serial-communication links, directly from the Inmos Transputer, which SGS-Thomson acquired in 1989. These links can

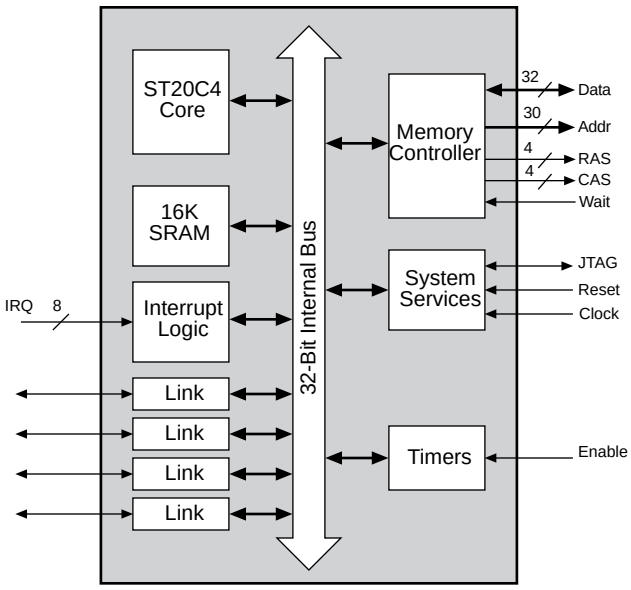

Figure 1. SGS-Thomson's ST20450 includes a mixture of general-purpose I/O devices with its on-chip SRAM and 32-bit ST20 core.

act as serial DMA controllers or communications channels and can even be used to boot the processor.

Each of the ST20450's four links pairs an input pin and an output pin. Each signal pin operates at a data rate of either 10 Mbps or 20 Mbps. One of the links has a slower, 5-Mbps rate, which is useful for booting the device serially or communicating with specially equipped logic analyzers. The simple link protocol is not synchronized with the processor clock and is insensitive to its phase, so multiple ST20450 chips can join their links as long as their clock speeds are all fairly similar.

The link pins have enough drive for short-haul communications of perhaps 4–6 inches—enough to cross a printed-circuit board but not far enough for remote devices. For board-to-board communication or longer transmissions, a matched 100-ohm transmission line with series matching resistors should be used. Serial-to-parallel converters are also available.

Memory Controller Fulfills Bus Duty

The ST20450 includes a 32-bit-wide DRAM controller in lieu of a conventional external bus interface. The controller drives RAS and CAS according to programmable timing parameters. Users can select the RAS-to-CAS delay as required to meet DRAM specifications. After a programmed delay, the ST20450 will read and latch data or present data on its data bus.

An input pin provides an opportunity for external logic to delay read or write cycles to DRAM subsystems that do not have consistent access times (for example, when memory is shared with another bus master). The '450 can also perform automatic CAS-before-RAS refresh cycles at programmed intervals.

The minimum cycle time for an external memory access is two clocks. At the ST20450's 50-MHz top speed, that's only 40 ns, so it is unlikely that many embedded systems would be able to take advantage of a full-speed memory cycle. The lack of a cache makes the on-chip SRAM necessary for a low-latency code store.

Processor	ST20450	Mantis	68340	i960JF
Frequency	50 MHz	30 MHz	25 MHz	33 MHz
Cache	None	None	None	4K/2K
SRAM	16K	None	None	1K
Memory ctrl?	Yes	Yes	No	No
Timers	2	5	2	2
DMA	None	1	2	None
Serial I/O	4	2	2	0
PCMCIA?	No	Yes	No	No
Data bus	32 bits	32 bits	16 bits	32 bits
Inst length	8–32 bits	32 bits	16–48 bits	32 bits
Package	PQFP-208	PQFP-208	CQFP-144	PQFP-132
Price (10K)	$35	$34	$31	$38

Table 1. The ST20450 is the first incarnation of the new ST20 core. In features and capabilities, it is competitive with chips such as GEC Plessey's Mantis (ARM), Motorola's 68340, and Intel's 960JF.

Price & Availability

The 3.3-V version of the ST20450 is sampling now at 50 MHz; production will follow in 4Q95. A 5-V version will follow by a few months. In 10,000-unit quantities, the 3.3-V, 50-MHz ST20450 is priced at $35. For more information, contact SGS-Thomson Microelectronics (Lincoln, Mass.) at 617.259.2500; fax 617.259.4420 or contact SGS-Thomson (Rousset Cedex, France) at +33 42.25.89.26; fax +33 42.25.89.93.

Seeking Out New Target Markets

SGS-Thomson clearly has an optimistic outlook on the demand for 32-bit microprocessors to have gone to the considerable trouble of developing its own. The C1, C2, and C4 cores are all similar and software compatible, as opposed to National's differently sized and mutually incompatible Piranha cores. The three cores will help SGS-Thomson attack three different price/performance areas.

At the low end, the company would like to secure printer designs. The midrange parts are targeted at GPS receivers and television set-top boxes, while the upper end of the ST20 family, including the ST20450, is intended for networking, ATM, and ISDN equipment, as well as wireless telecomm applications. Table 1 compares the '450 with some similarly priced CPU chips.

A planned low-power derivative of the C1 core, called C0, will be attractive for battery-powered applications like PCMCIA cards, and it may replace the C1 core within a short time. Such parts will compete with GEC-Plessey's recently announced Butterfly, Spider, and Mantis controllers *(see **090902.PDF**)*. The ARM-based chips have broader software and tool support, but without the Thumb unit, they do not approach the code density of the new ST20-based devices.

SGS-Thomson has made a bold move by developing an architecture that it must support on its own. Early adopters will have to rely on the compiler, assembler, and debugger supplied by the company. Third-party support, for the time being, is nonexistent. It remains to be seen how many new microprocessor designs the industry can digest before some start falling away, relegated to shrinking niches or disappearing completely.

On the other hand, new applications are discovered almost daily, and some designers have found that a processor with a desktop pedigree simply does not offer the right mix of performance, power consumption, and code density that they require. NEC, Hitachi, ARM, Motorola, and others have stepped into this void with CPUs specifically for embedded applications. SGS-Thomson, for one, hopes that there are a number of engineers who have not yet found what they are looking for. ♦

