Literature Watch

ASICs

CICC '95 bares the latest in ASICs. May's Custom Integrated Circuits Conference covers digital, analog, and communications chips. Lisa Maliniak, et al; *Electronic Design,* 5/1/95, p. 63, 21 pp.

Buses

Bus logic refuses to die. Descendants of the original 7424x TTL chips keep coming long after most MSI chips have disappeared. Rodney Myravaagnes, *Electronic Products,* 5/95, p. 29, 2 pp.

Secret PlugFests let board vendors PnP. The Plug and Play Association holds occasional gatherings to verify that cards and systems work together. Stephan Ohr, *Computer Design,* 5/95, p. 28, 2 pp.

Development Tools

Simulation backplanes allow concurrent use of multiple simulators. Like hardware-backplane standards PCI and SCSI, standard simulation backplanes allow you to connect multiple simulators for substantial gains in design productivity. Kevin Jorgensen and Peter Odryna, Precedence; *EDN,* 5/11/95, p. 165, 5 pp.

AHDL tools emerge before standards are realized. Early versions of analog hardware description languages (AHDLs) have generated criticism and controversy. Stephan Ohr, *Computer Design,* 5/95, p. 36, 6 pp.

Rules-based tools help designers with deep-submicron ICs. At 0.5-micron and below, it is critical to link logical-design and physical-design tools. Mike Donlin, *Computer Design,* 5/95, p. 46, 3 pp.

Signal-crafting tool controls IC timing and noise problems. Cooper & Chyan's IC Craftsman handles physical layout for both digital and analog ICs in deep submicron technologies. Lisa Maliniak, *Electronic Design,* 5/1/95, p. 167, 2 pp.

EMI modeling pushes prototypes past test. For systems that run faster than 50 MHz, EMI modeling tools can help designers meet strict guidelines. Mike Donlin, *Computer Design,* 5/95, p. 32, 2 pp.

Design-rule checks help users create complex layouts. Design-rule checking (DRC) can greatly simplify a board layout when a user defines design requirements at the start of a project, but it's also important to define and refine data and rules throughout the entire design process. Russ Lindgren, *Personal Engineering,* 5/95, p. 24, 5 pp.

DSPs

EDN's DSP-chip directory. One-page descriptions of nearly two dozen current DSP chips and cores. Markus Levy and James P. Leonard, *EDN,* 5/11/95, p. 40, 25 pp.

DSPx '95 product review. Highlights from the recent trade show covering DSP products and tools. Steven H. Leibson, *EDN,* 5/11/95, p. 99, 5 pp.

Memory

DRAMs take on features to match blazing CPU speeds. System makers now face a wide range of choices in memory architectures as chip suppliers attempt to set new standards. Robert Ristelhueber, *Electronic Business Buyer,* 5/95, p. 33, 4 pp.

Miscellaneous

High-performance ADCs are pipelining. First there was the SAR, then flash-based multipass architectures, but the baton has now been passed to pipelines. Frank Goodenough, *Electronic Design,* 5/15/95, p. 91, 6 pp.

Fuzzy, neural and genetic methods train to overcome complexity. Emerging from academia into the real world, fuzzy logic, neural networks, and genetic algorithms are able to complement each other's strengths and compensate for disadvantages. Tom Williams, *Computer Design,* 5/95, p. 59, 9 pp.

64-Gbit DRAMs, 1-GHz microprocessors expected by 2010. The SIA projects that, by 2012, CPUs will measure 620 mm^2 in 0.07µ CMOS and use 1,000-pin packages. Ray Weiss, *Computer Design,* 5/95, p. 50, 2 pp.

Processors

Turning back the clock. In spite of some critics, several microprocessor vendors are investigating asynchronous circuits for part or all of a processor design. W. Wayt Gibbs, *Scientific American,* 6/95, p. 40, 1 pg.

Programmable data paths speed computations. With four programmable macrosequencers, the RAD5A4 programmable arithmetic data-path chip, developed by Infinite Technology, has a throughput of up to 400 million 16 × 8-bit multiply-accumulates per second. Dave Bursky, *Electronic Design,* 5/1/95, p. 171, 3 pp.

Programmable Logic

Advanced 100-kgate FPGA family takes on gate arrays. High-gate-count flash-base FPGAs pack 100,000 gates and rival the ease-of-use of gate arrays. Dave Bursky, *Electronic Design,* 5/1/95, p. 51, 4 pp.

Detailed model shows FPGAs' true costs. Design decisions are far more complex than simply weighing the unit price and NRE charge to determine whether to use FPGAs or ASICs. Joseph Liu, Xilinx; *EDN,* 5/11/95, p. 153, 4 pp.

System Design

Making the bare-die decision. Here's how to determine whether or not to take the wraps off of the ICs in your next design. Jim Schrand and Rick Ried, Intel; *Electronic Design,* 5/1/95, p. 129, 4 pp.

PowerPC climbs onto the VME. While the 68K dominates VME boards, RISC processors hold 25% of the market. Jeff Child, *Computer Design,* 5/95, p. 112, 9 pp.

