Literature Watch

ASICs

ASIC vendors struggle to differentiate their products. Some ASIC vendors are partnering with EDA vendors, others have embraced third-party tools, and still others are developing function-block libraries. Barbara Tuck, *Computer Design,* 2/95, p. 100, 5 pp.

What system designers need to know about deep-submicron ASICs. As device geometries slip below 0.5 µm, interconnect delays become much larger than gate delays, and transistors don't work the same way they did before. Isadore Katz, Meta-Software; *EDN,* 2/16/95, p. 69, 3 pp.

Deep-submicron ASIC design requires design planning. The effects of deep-submicron geometries, higher clock speeds, and soaring gate counts all create design problems existing tools do not address. Bob Wiederhold, High Level Design Systems; *EDN,* 2/16/95, p. 95, 4 pp.

Monster ASICs emerge from "deep submicron silicon." Semicustom chips with more than a million gates of logic require users, suppliers, and design-automation vendors to work together more closely. Robert Ristelhueber, *Electronic Business Buyer,* 2/95, p. 39, 3 pp.

Development Tools

Graphical capture tools port designs to HDL code. Graphical front ends simplify the use of hardware design languages such as Verilog and VHDL. Russ Lindgren, *Personal Engineering,* 2/95, p. 35, 7 pp.

Functional simulation helps maintain PLD designs and also checks design-tool output. Complex PLDs should be functionally simulated using both expected and unexpected conditions. Lance Fisher, Intellimetrics, *Personal Engineering,* 2/95, p. 52, 5 pp.

DSPs

Consumer applications drive DSP evolution. A directory of DSP chips. John Mayer, *Computer Design,* 2/95, p. S44, 4 pp.

Grape-11: a system-level prototyping environment for DSP applications. Grape-11 has been used successfully in three real-world DSP applications to reduce programming effort and minimize development cost. Rudy Lauwereins, Marc Engels, et al, Katholieke Universiteit Leuven; *IEEE Computer,* 2/95, p. 35, 9 pp.

Memory

Intel flash devices offer flexible mapping, noncontiguous memory spaces. Intel's 28FxxxBX flash memories offer a write-lockable boot block and writable EEPROM code and data spaces. Jim Kelsey, *Personal Engineering,* 2/95, p. 59, 4 pp.

Faster processors ignite SRAM revolution. A directory of specialty SRAMs. (Other sections cover high-performance DRAM, EPROMs, serial EEPROMs, and flash memory.) Jeffrey Child, *Computer Design,* 2/95, p. S48, 5 pp.

High-density flash memory now a practical option for system design. As densities increase, prices drop below the cost of DRAM, and manufacturers enhance performance, flash memory is gaining momentum. Markus Levy, *EDN,* 2/16/95, p. 53, 7 pp.

Miscellaneous

Ubiquitous mobile communications. Wireless telephones, pagers, and other devices are being tied together on land and through satellites. Larry Marion, *Electronic Business Buyer,* 2/95, p. 46, 6 pp.

Processors

RISC matures into mainstream. A directory of RISC processors. Jeff Child, *Computer Design,* 2/95, p. S36, 7 pp.

Programming the TPU. This overview shows you how to get started on projects using Motorola's versatile Time Processor Unit. Eric McRae, *Embedded Systems Programming,* 3/95, p. 22, 12 pp.

Programmable Logic

Face-off: benchmarking FPGAs and CPLDs. The chairman of PREP and the CEO of Exemplar debate the merits of standardized synthesis benchmarks. Rita Glover, EDA Today; *Computer Design,* 2/95, p. 97, 3 pp.

System Design

Designers stretch to meet low-voltage system demands. The 30-year-old world of standard 5-V design has shifted into a mixed-voltage landscape, with 3.3-V and lower voltages becoming mainstream design standards. Ray Weiss, *Computer Design,* 2/95, p. 61, 9 pp.

Design considerations bring unity to a mixed-voltage world. If you design with low-voltage devices, you've probably encountered the compatibility issue of making systems operate with some 5-V devices. Kenneth M. Cuy, AMD; *EDN,* 2/2/95, p. 115, 3 pp.

Onboard regulators. Distributing power in board-based systems is a complex equation involving economics, real-estate constraints, thermal issues, EMI and RFI, and regulator performance. Bill Travis, *EDN,* 2/16/95, p. 34, 8 pp.

Vertical processing systems: a survey. After reviewing the characteristics of various commercial and research models such as the DAP, MPP, and CM, this survey proposes a combined architecture that links a VPS with a set of highly specialized, homogenous coprocessors. Yakov I. Fet, Russian Academy of Science; *IEEE Micro,* 2/95, p. 65, 11 pp.

A smorgasbord of clock chip solutions. Manufacturers exploit a variety of technologies to get signals to their destination on time. Even entry-level PCs require careful attention to clock management, and vendors try to ease the task. Rodney Myrvaagnes, *Electronic Products,* 2/95, p. 33, 3 pp.

