NEC Plunges into PDA Processor Market

R4100 Chip Offers Very Low Power Consumption

by James L. Turley

Extending its MIPS-based microprocessor product line at the low end, NEC has developed a new 64-bit implementation aimed directly at mobile computing applications. The new R4100 delivers 45 Dhrystone MIPS at 40 MHz, placing it in the thick of recently announced chips from Toshiba, IDT, ARM, and others. The new chip boasts a multiply-add instruction and exceptionally low power consumption; both features are calculated to appeal to designers of handheld equipment like PDAs, organizers, and personal communicators.

The R4100 will be offered exclusively by NEC. It is only the second MIPS chip the company has designed itself, the first being the R3800, which is marketed only in Japan. First samples of the new chip should be available in the middle of the year, with general availability near the end of 1995.

New Chip Based on R4200

Unlike some other recent embedded MIPS chips, the R4100 is truly an R4000-series implementation. It has a 64-bit register set and supports all the MIPS-III instructions, including conditional traps and branches and 64-bit arithmetic.

The R4100 is descended directly from the MIPS 4200 *(see **070701.PDF**)*, with enhancements that make it more suitable for embedded systems, where heat and power dissipation become important considerations. Both parts have identical MMUs and a TLB with 32 double entries. Both share a five-stage pipeline and single-cycle execution. The 4200's unusual unified integer/floating-point data path has been simplified to save space, leaving a conventional 64-bit integer core.

The R4100's major structural addition over its predecessor is a new multiply-add instruction, a stab at displacing integer DSP chips for telecommunications applications and an increasingly popular enhancement to many microprocessors. The new instruction boasts single-cycle throughput. Pipelining a stream of them could deliver a peak rate of 40 million $16 \times 16 + 64 \rightarrow 64$-bit multiply-add instructions per second—ample performance for a virtual modem, audio synthesis, or video-game acceleration.

A 2K instruction cache and a 1K data cache isolate the processor from memory latency, but they are quite small for a 64-bit RISC processor with a rapacious appetite for instructions. Both caches are direct mapped. On a miss to either cache, the pipeline stalls until all four words are loaded into the cache line. Updates to the data cache use the write-back protocol.

The caches are both virtually indexed, allowing them to perform address translation in parallel with the cache access. Physically tagging the caches allows them to remain consistent with external memory when the R4100 shares the bus with another master.

Although the R4100 has a 64-bit core, its external data bus is only 32 bits wide and is multiplexed with the address bus. The bus runs at 1× or 1/2× the frequency of the processor core, reducing power consumption, lowering electromagnetic emissions, and simplifying interfacing. The limited bandwidth of the slow, narrow bus will have a tangible impact on performance, however.

The standard MIPS-style SysAD bus is normally a difficult one to interface with external logic, but the torpid 20-MHz frequency should ease that task considerably. The 36-bit multiplexed bus and the six control signals both carry parity bits, which can be disabled if desired. All transactions are synchronous, with a three-cycle minimum latency. Both big- and little-endian byte ordering are supported.

Low Power Consumption Sets R4100 Apart

The R4100's performance/power ratio is head and shoulders above the rest of the current crop of embedded microprocessors. Judging by the much-abused Dhrystone 1.1 benchmark, the R4100 delivers 45 MIPS at 40 MHz. That speed is achievable only at 3.3 V, where

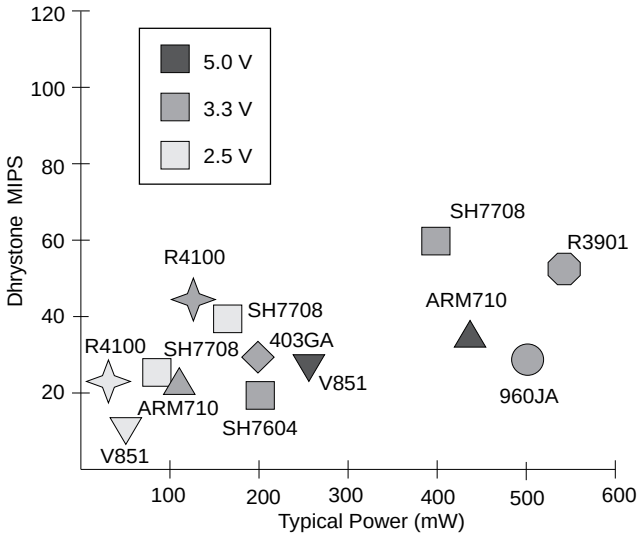

Figure 1. A comparison of low-power embedded microprocessors shows NEC's R4100 leading the pack in MIPS/watt (50-pf load).

power dissipation is a mere 120 mW, even with a 50-pf bus load. The resulting 375 MIPS/watt ratio places the R4100 far ahead of any currently shipping part. Of course, the R4100 itself is not expected to begin shipping until near the end of 1995.

Turning the voltage down to the part's 2.2-V lower limit decreases the maximum clock frequency to 20 MHz. The power consumption drops precipitously to only 27 mW. At this voltage, the R4100 should deliver an amazing 815 MIPS/watt.

Like most new embedded chips, the R4100 has multiple power-conservation modes. Standby mode halts all internal processing activity, but the bus interface continues to operate. Suspend mode also stops bus activity. These two modes drop power consumption by 90% and 95%, respectively. Any external interrupt will wake the R4100 within a few clock cycles.

Hibernation mode shuts down the entire processor, including the internal PLL, caches, and interrupt logic, and reduces current draw to just microamps. Only a hard reset can resurrect the chip from hibernation; all processor state is lost. This mode serves as a way to effectively turn the processor off and remove it from the circuit without actually shutting off system power.

Low-Power Device Just the Beginning?

To some extent, the impressively low power numbers are no surprise. NEC bought its way into the winner's circle with its 0.5-micron three-layer-metal CMOS process (which the company calls 0.35 micron, based on effective gate length). This process, similar to the one NEC uses for its 200-MHz R4400 desktop engine, is aggressive for such a low-cost microprocessor. The process has been proven, suggesting that R4100 production should not be held up with last-minute manufacturing delays.

The R4100's performance level positions it well below the R4200, leaving a big gap between the two chips in NEC's product line. Clearly, the R4100's clock speed is not limited by its process or by its core design but instead is being paced to keep power consumption down to a manageable minimum.

That leaves an opening for another R4200 derivative, perhaps in the guise of MIPS Technology's upcoming C1 design *(see **0903MSB.PDF**)*. With a faster multiplier and a more workable bus interface, a 100-MHz "R4300" would be attractive for higher-performance line-powered units. Such a future chip would also be ideal for Nintendo's upcoming Ultra64 (aka Project Reality) game player *(see **0810MSB.PDF**)*.

The R4100 is a tiny chip, with a die that measures a mere 5 mm on a side. The MDR Cost Model places the manufacturing cost of the part at about $8, comparable with ARM and SH parts and about right for NEC's expected $25 volume price. The part will be housed in a 100-lead TQFP.

Price & Availability

Engineering samples of the 40-MHz R4100 will be available in June, with general availability scheduled for 4Q95. Sample pricing is $50; the price for large volumes (quantities of 100,000 and up) is expected to be about $25. For more information, contact NEC Electronics (Mountain View, Calif.) at 800.366.9782; fax 415.965.6130.

Good Fit for Small Handheld Applications

NEC's new chip comes out amid a flurry of new MIPS chips and cores from IDT, Toshiba, and LSI Logic, many of them with similar enhancements aimed at promoting the chips for mobile and consumer applications.

As Figure 1 shows, the R4100's nearest neighbors in the MIPS/watt race are mostly 16-bit SH chips and NEC's own V800 series. Hitachi's newest SH7708 *(see **090302.PDF**)* makes the best comparison: at 2.5 V, the SH7708's power consumption and Dhrystone rating are comparable to those of the 3.3-V R4100. the Dhrystone benchmark, unfortunately, fits into the R4100's 2K cache; the SH7708's larger 8K cache will help it considerably in practical applications. The SH7702, which comes with a 2K cache, would deliver identical Dhrystone MIPS but draw even less current.

Toshiba's R3901 *(see **090205.PDF**)* makes an interesting contrast. The chips perform comparably on Dhrystone at similar speeds, but the R3901's separate caches, debug support module, and demultiplexed bus contribute to its much greater power consumption.

Although the R4100 is clearly intended for handheld PDA-type applications—NEC has said as much—the company is not announcing any plans to port PDA operating systems to the R4100. That begs the question of who will use the chip and what software it will run. It is unlikely that Apple, which already supports ARM and has a stake in PowerPC, would be willing to take on a third architecture for its Newton operating system.

That situation makes Magic Cap the obvious contender. General Magic has already stated that it is porting its OS to at least one unnamed processor architecture *(see **090204.PDF**)*. Given that Toshiba, another MIPS licensee, will be supplying ASICs to General Magic, it seems clear that MIPS has made General Magic's short list. If other manufacturers join Sony and popularize Magic Cap devices, there could be a significant upside for embedded MIPS vendors like NEC.

In the expanding consumer electronics and handheld computer markets, leadership is measured not in MIPS, SPECint, or MFLOPS but in increasingly low energy consumption. To win in these high-volume embedded applications, the lack of power is a key to success. ♦

