Literature Watch

Buses

Implementing DMA support for PCMCIA. DMA will soon become a part of the growing PCMCIA feature set on both PC Cards and host systems. Sanjiv Pathak, Gary Gildersleeve, Cirrus Logic; *IC Card Systems & Design,* 11–12/94, p. 39, 3 pp.

PCI bus speeds peripheral communications. The PCI bus is a high-speed highway, but on-ramps in the form of off-the-shelf, general-purpose PCI I/O controller chips are few and far between. John Gallant, *EDN,* 12/8/94, p. 93, 5 pp.

Development Tools

A/D simulators: an expanding array of choices. Various options are available when planning to simulate designs that mix analog and digital circuitry. Lisa Maliniak, *Electronic Design,* 12/5/94, p. 95, 6 pp.

DSPs

TI chips dominate DSP coprocessor boards, I/O migrates offboard. A brief survey of DSP chips and boards that are currently available. Paul G. Schreier, *Personal Engineering,* 12/94, p. 37, 10 pp.

Graphics

Draw workstation graphics into mainstream PCs. A graphics design based on the traditional VGA architecture cannot begin to handle the data-transfer bandwidth required for such high-resolution, true-color, high-refresh-rate displays. Rhett Saugier, AT&T Microelectronics; *EDN,* 12/8/94, p. 131, 9 pp.

Memory

Are multiport memories physically feasible? At least for small (≤16K) devices, the answer is yes. Two possible structures are presented. Martti J. Forsell, University of Joensuu, *Computer Architecture News,* 12/94, p. 3, 8 pp.

Flash memory metamorphoses into DRAM designs. Flash chips are beginning to displace DRAM for some code-storage applications. Jeff Child, *Computer Design,* 12/94, p. 38, 3 pp.

Miscellaneous

Windows NT challenges UNIX for embedded and real-time development. As a desktop computing, programming, and development environment, Microsoft's Windows NT operating system is a serious contender to UNIX. Tom Williams, *Computer Design,* 12/94, p. 47, 5 pp.

Digital video spearheads TV and videoconferencing applications. Both set-top boxes and multimedia PCs will require specialized silicon for MPEG video decompression. Stephan Ohr, *Computer Design,* 12/94, p. 59, 9 pp.

Optical neural chips. Mitsubishi researchers built an artificial retina from two GaAs chips, combining optical devices with a neural network. Eberhard Lange, Yoshikazu Nitta, Mitsubishi Electric; *IEEE Micro,* 12/94, p. 29, 13 pp.

PDAs: what will it take to satisfy users? The biggest obstacles to acceptance are the user interface, software applications, and connectivity. Clifford Meth, *Electronic Design,* 12/16/94, p. 49, 4 pp.

Technology 1995: large computers. In the past year, multiprocessor UNIX systems hit the big time while mainframes muddled on and supercomputers flopped. Gerry Khermouch, *IEEE Spectrum,* 1/95, p. 48, 4 pp.

Innovation delayed is innovation denied. The Vice President of the United States discusses federal policy for the communications market. Al Gore, U.S. Government; *IEEE Computer,* 12/94, p. 45, 3 pp.

Peripherals

ATM switching: a brief introduction. An overview of the scalable, switched structure of asynchronous-transfer-mode (ATM) networks. Lee Goldberg, *Electronic Design,* 12/16/94, p. 87, 10 pp.

LAN and I/O convergence: a survey of the issues. Once two distinctly separate technologies, LANs and I/O are becoming more alike through similar distances, media, and purposes. Martin W. Sachs, Avraham Leff, et al, IBM; *IEEE Computer,* 12/94, p. 24, 9 pp.

Processors

Intel and Philips launch supercharged 8051 architectures. Intel's MCS 251 and Philips 80C51XA extend the popular 8051 in different ways. Ray Weiss, *Computer Design,* 12/94, p. 30, 2 pp.

Source list: 16-bit microcontrollers. A survey of currently available 16-bit embedded processors. *Electronic Products,* 12/94, p. 38, 4 pp.

Programmable Logic

FPGA macros simplify state machine design. Try this one-hot-encoding macro-based approach when implementing state machines in flip-flop-rich architectures such as FPGAs. Jeffrey V. Preston, John D. Lofgren, Martin Marietta; *Electronic Design,* 12/5/94, p. 109, 6 pp.

System Design

Embedding microprocessor cores and complex functional blocks in ASICs. If your goal is to build a system-on-a-chip, today's short design cycles mandate the integration of complex functional blocks with RISC microprocessor or DSP cores. Christian Joly, *Computer Design,* 12/94, p. A26, 3 pp.

History cache: hardware support for reverse execution. An alternative to the reorder buffer in out-of-order processors. Rok Sosic, Griffith University, *Computer Architecture News,* 12/94, p. 11, 8 pp.

