

At a Glance

AMD's K5 Designed to Outrun Pentium	1
AMD's forthcoming Pentium-class processor, code-named K5, takes a radically different approach: caching predecoded x86 instructions and converting them into "RISC operations" that are executed in an advanced superscalar core. The chip, which should be clock-for-clock faster than Pentium, could outperform the fastest Intel processors and is due to ship around the middle of next year.	
Editorial: Coming Next Year—586 vs. 586	3
With a number of vendors offering x86 processors, the traditional naming scheme is breaking down, engendering buyer confusion. New, widely accepted benchmarks could resolve these problems.	
Most Significant Bits	4
TI's Rio Grande runs dry; Intel slashes Pentium, 486 prices; PowerPC 604 announced at 100 MHz; Motorola deploys first PPC 603 systems; Toshiba endorses PowerPC; Judge rules for Intel on ICE microcode; Philips buys HDL, MIPS license.	
620 Fills Out PowerPC Product Line	12
The PowerPC 620, the first 64-bit implementation of PowerPC, will boost high-end performance by 40% over the 604 and offer additional enhancements aimed at servers, increasing memory bandwidth and reducing branch latency. These enhancements have significantly increased die size and cost over the 604.	
MIPS R10000 Uses Decoupled Architecture	18
Another next-generation RISC, the R10000, could allow the MIPS line to challenge the performance leaders when the chip begins shipping late next year. Its speculative and out-of-order micro-architecture, which decouples instruction issue from execution, is the most aggressive yet revealed.	
AMD Unveils First Superscalar 29K Core	23
AMD's first new 29K core since 1988 brings the sophisticated out-of-order techniques used by its big brother, the K5, and other next-generation RISC designs to the embedded world. Expected to ship by mid-1995, the new chips will challenge Intel's 960 H series for high-end embedded design wins.	
Motorola Redefines 68K Instruction Set	27
Aiming to fend off the new embedded RISCs, Motorola has developed a low-cost core, dubbed ColdFire, that implements a revised version of the 68K instruction set. By breaking binary compatibility to streamline the architecture, new devices promise 68040 performance at 68000 prices.	
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