Most Significant Bits

Intel Preps 75-MHz Pentium for Notebooks

Although the official announcement won't be until fall, Intel has begun to reveal information about a program to put Pentium chips into notebook PCs using a new version of the P54C processor that operates at 75 MHz. This clock speed offers some power reduction from the 90- and 100-MHz parts and, with a new 3× clock mode, allows the system bus to operate at the 25-MHz rate popular in notebook designs, although a different motherboard is required for Pentium's 64-bit bus.

At 75 MHz, the maximum power dissipation of the chip remains a daunting 7 W, but the power-management features built into the P54C *(see **080301.PDF**)* can reduce average power dissipation to around 3 W, similar to a 50-MHz 486DX2 or 100-MHz DX4. Because battery life is determined by the average continuous power, not the maximum power, the battery in a 75-MHz Pentium notebook should last about as long as in current DX2 models.

Intel has been distributing samples of Pentium chips using a TAB package, and it is likely that the notebook Pentium will use this package to reduce board area and cost. The 75-MHz Pentium has too many pins and dissipates too much power for an inexpensive PQFP, but the TAB package *(see **071304.PDF**)* should be adequate to cool the chip if the system board is properly designed. (TAB devices typically use ground planes in the PC board as heat sinks.)

The company would not comment on price or availability of the 75-MHz part. Sources indicate that the frequency yield on the P54C is very good at 90 MHz, so adding a lower speed grade would do little to reduce Intel's manufacturing costs. The lower cost of the TAB package could allow Intel to offer a price break on this part, or the company could simply charge the same as for a 90-MHz Pentium (which, apart from the new package, the part essentially is) and pocket the extra profits.

We expect Intel's notebook lineup, by the end of the year, to feature the 50-MHz SX2 at the low end, the 75-MHz DX4 in the midrange, and the 75-MHz Pentium at the high end. By that time, Intel's competitors may be able to match the DX4, but the new Pentium should have clear sailing in portable systems until at least mid-1995, when AMD and Cyrix begin shipping competitive chips in significant volumes.

Cyrix Wins Contract with AST

Exposing another chink in Intel's armor, Cyrix has won a major contract with PC vendor AST Research. This is the first time a top-tier PC vendor has selected Cyrix, which previously counted Epson and Zenith as its biggest wins. Neither company is willing to discuss which processor models are involved; one possibility is Cyrix's unique 80-MHz 486DX2 combined with access to the future Pentium-class M1 processor.

Cyrix's foundry deal with IBM undoubtedly helped convince AST to work with the diminutive CPU vendor. Compaq's agreement to use AMD processors may have also made it easier for AST to accept non-Intel processors. Like Compaq, however, AST will continue buying the bulk of its CPU chips from Intel. The win provides a big boost for Cyrix and shows that the Intel Inside campaign has failed to generate enough end-user preference to keep Intel's biggest customers in the fold.

NKK Announces R4600 Processor, Chip Set

Emerging from the shadows, Japanese vendor NKK has announced that it will become the third source of the MIPS R4600 processor, joining IDT and Toshiba. The company says that it will sample by September a 100-MHz R4600 that operates at 3.3 V and will begin volume shipments in 1Q95.

NKK contributed funding to the development of the R4600, a fact only recently made public. It intends to produce a 150-MHz version, also at 3.3 V, by mid-1995. All of IDT's R4600 parts operate at 5 V, but Toshiba is shipping a 3.3-V part at 100 MHz.

NKK also announced a system-logic chip set that connects the R4600 to a secondary cache, main memory, and PCI. The two-chip set operates at 3.3 V but supports 5-V memory chips and PCI devices. It can handle up to 1M of secondary cache and up to 256M of DRAM. NKK offers a design kit, called Aquarius, that includes the R4600 processor, PCI chip set, and a PCI-to-ISA bridge for access to standard PC peripherals.

No pricing is available on any of these products, making it difficult to compare them to similar devices from other vendors. It isn't clear that the world needs a third R4600 supplier. The PCI chip set, which also supports other R4x00 processors, fills a gap in the MIPS chip set lineup, but NKK joins Acer, Deskstation, NEC, and Toshiba in competing for a vanishingly small market for MIPS-based PC designs.

MTI Develops R4x00 for Pentium Socket

MIPS Technologies (MTI) has announced a design kit, carrying the unfortunate name of UltraP, that allows an R4x00 processor to plug into a Pentium socket. The kit lets vendors create custom daughter cards that contain a MIPS processor, a socket for the Pentium chip, and an ASIC that converts the R4x00 bus protocol into the Pentium bus protocol.

The concept is that users can remove the socketed Pentium processor from their system, plug it into the

UltraP board, and put the whole assembly back into the CPU socket on the motherboard. The system then boots using the Pentium processor, eliminating the need for the MIPS chip to emulate the x86 boot code. Once the system is booted, the user can engage Windows NT on the R4x00. With current software, there is no way to toggle between the x86 and MIPS processors, but MTI promises this capability in a future release.

MTI is offering this design free of charge to any PC vendor. The incremental cost of an UltraP board with a 100-MHz R4600 process is about $365, according to MTI. So far, no PC vendors have announced plans to build systems or upgrade cards using the UltraP design.

MTI claims that a 100-MHz R4600 delivers "up to" 2.3 times the performance of a 60-MHz Pentium processor on some Windows NT applications, but it gave no information on what the average improvement might be. Based on SPECint92, the R4600 is only slightly faster. Again using SPECint92, a 90-MHz Pentium delivers nearly the same performance as the fastest MIPS processors shipping in volume today. Once one has already paid for a Pentium, it seems like a waste to use it as a boot processor; without the switching software, potential customers are those who only use applications that run faster on the MIPS processor than on a Pentium.

The upgrade board could foreshadow a MIPS processor with on-chip x86 emulation *(see **080704.PDF**)*; such a device could replace the UltraP board by plugging directly into the Pentium socket. To do so, the chip would have to support a direct Pentium bus interface, eliminating the need for PC vendors to make motherboard changes to accommodate the RISC chip. IBM's rumored PowerPC 615 is said to incorporate a Pentium bus interface and Pentium pinout for this reason.

Letter to the Editor

In your article "Room for Three Architectures in the 2000s" *(see **0809VP.PDF**)*, the author misses a basic point: Intel no longer has control of the instruction set. The instruction set is determined by the installed base of PC applications and by which set of x86 instructions Microsoft (and other PC compiler vendors) chooses to support.

Secondly, the article misses the major issue of where in the march to 100+ million transistor chips does a new architecture make sense? Optimal architectures will change as one goes from less than 5 million transistors per chip to the 5–50 million transistor range. Maybe another change will be warranted above that number. Even if Intel/HP have control of the "desktop PC" instruction set (which they don't), where in this progression is VLIW optimal? What is the optimal design point for the year 2000 in millions of transistors and what is the optimal architecture for that design point?

I would agree with the author that a smaller number of companies will have the ability to marshall the resources—semiconductor process, money, expertise—to design microprocessor architectures and even fewer companies will have the ability to influence their acceptance in the market. Unless, as history has repeatedly proven, innovative companies come up with clever strategies to use market forces to their advantage.

—Vinod Khosla, Kleiner Perkins Caufield Byers
(a major investor in NexGen)

Nintendo Selects Rambus

Rambus has announced its first major public design win: Nintendo's next-generation, 64-bit video game, called the Ultra-64 (also known as Project Reality). Promised for a 4Q95 introduction, the video game will use an R4200-derivative microprocessor, a single 16-Mbit RDRAM, and an ASIC, resulting in a design streamlined enough to sell for its intended retail price of less than $250.

This application highlights the greatest strength of Rambus: it can deliver its full bandwidth from a single device, reducing the minimum memory size to one chip. The game will use semiconductor memory cartridges, not CD-ROMs, because they enable much faster response and reduce the cost of the basic system. (These cartridges, however, will not match the storage capacity of a CD-ROM.)

The Nintendo win removes some of the uncertainty over whether RDRAM volumes will be high enough to drive prices down. Assuming that Nintendo is able to shift its existing game market to the new system, this one application could account for sales of more than five million RDRAMs per year. The next big metrics for Rambus are the number of graphics controllers introduced with RDRAM interfaces, and how these chips compare to those supporting the MoSys devices *(see **081002.PDF**)*. In the long run, Rambus will also have to make inroads in main memory to achieve the company's goals, while MoSys has more modest goals. Small systems like Nintendo's, which use a single memory for both graphics and data, may be one of Rambus's biggest opportunities.

Number Nine Ships 128-Bit Graphics Chip

Following the same route as ATI *(see **061301.PDF**)*, graphics-board vendor Number Nine has developed its own graphics accelerator chip, the Imagine 128 (I-128). As the name suggests, the chip includes a 128-bit graphics engine, the first to achieve this milestone, and supports either a 64- or 128-bit path to the graphics frame buffer. In the latter configuration, the I-128 can deliver 500 Mbytes/s of bandwidth to a VRAM frame buffer.

The chip uses a "triple-buffer" design to support complex animation and video applications. In addition to the VRAM frame buffer, a DRAM backing store can be used for off-screen pixel maps or for double-buffering an-

imation frames. A third memory area creates a small moveable window for video images.

The I-128 connects directly to PCI with its host-bus interface. The chip also contains a direct ISA interface, allowing it to deliver glueless VGA emulation in DOS-based systems. Number Nine plans to develop drivers for Windows, NT, and other operating systems, and will support PowerPC along with x86 processors.

The company rates its chip at 155 WinMarks (version 3.11) or 55 WinMarks (version 4.0) in a 100-MHz Pentium system, outrunning all other graphics accelerators. The high bandwidth delivers strong performance even in 16- and 24-bit color modes. The design is so fast that it is really not appropriate for most PC users, even for entry-level Pentium systems. It really hits its stride with today's fastest PCs and will last through the lifetime of Pentium and even into early P6 systems.

The chip is now sampling; Number Nine expects to ship the I-128 in 4Q94 at $160 in 10,000-unit quantities. Although this price is reasonable for the level of performance provided, it places the chip out of the volume portion of the market. ♦

