Literature Watch

ASICs

Submicron ASIC tools enhance predictability. Accurate delay models and tight links between synthesis and layout produce ASIC designs that work. Lisa Maliniak, *Electronic Design,* 4/18/94, p. 61, 5 pp.

Development Tools

One-box test system does it all. Stimulus, response, and analysis in one highly integrated system make design verification faster and less expensive. John Novellino, *Electronic Design,* 5/2/94, p. 125, 2 pp.

On-chip debug: panacea? No. Useful? Yes. More and more debug capability is being brought on board the processor rather than relying on external hardware. Dan Strassberg, *EDN,* 4/14/94, p. 71, 6 pp.

CPLD module packs 50K usable gates, 360 I/O pins. A multichip module for emulating and prototyping ASICs combines four CPLDs packing 50,000 gates and 360 I/Os into a single package. Dave Bursky, *Electronic Design,* 4/4/94, p. 45, 3 pp.

DSPs

Mainstream applications require optimized assembly language for fast DSPs. To take advantage of DSP's speed requires recompiling and sometimes hand-optimizing your code. John P. Sweeney, AT&T Microelectronics; *EDN,* 4/28/94, p. 77, 5 pp.

MPUs lead emulators on wild chase. Emulator vendors struggle to keep pace with escalating microprocessor complexities and speeds, while price cutting squeezes the market's value. Dwight B. Davis, *Electronic Business Buyer,* 4/94, p. 135, 4 pp.

Miscellaneous

Setting sun: the slide of Japanese semiconductors. Japanese companies' emphasis on a small range of high-volume commodity products may prove to be a faulty strategy. Robert Ristelhueber, *Electronic Business Buyer,* 4/94, p. 52, 7 pp.

Coming to grips with compression. Comparing the various software-only and hardware-based compression schemes shows the future of multimedia and set-top boxes. Bernard C. Cole, *OEM,* 4/94, p. 28, 6 pp.

Washington opens up to convergence. Lawmakers are beginning to notice the coming revolution in telecommunications. Their decisions will shape the future information superhighway. George Leopold, *OEM,* 4/94, p. 49, 5 pp.

Silicon, analog processes are becoming more sophisticated. High-performance complementary bipolar and bipolar/CMOS processes require greater designer knowledge. Frank Goodenough, *Electronic Design,* 5/2/94, p. 97, 6 pp.

Peripherals

ATM silicon: ready for takeoff. The complexity of the ATM standard and the need for short development cycles are forcing a high level of controller integration. Lee Goldberg, *Electronic Design,* 4/4/94, p. 51, 9 pp.

Processors

Wanted: low-cost, small 8-bit µCs to take on the dirty work. A directory of inexpensive yet effective 8-bit microcontrollers from 10 manufacturers. Ray Weiss, *EDN,* 4/14/94, p. 57, 6 pp.

System Design

Tips for straddling the 3-V to 5-V fence. Designers creating mixed 3-V and 5-V systems need to be familiar with a few basic issues to avoid future trouble. Brian C. Martin, Philips Semiconductors; *Electronic Design,* 4/4/94, p. 67, 6 pp.

Distributed power takes center stage. Systems that need flexibility in supply voltages and power levels can get big benefits from distributed power. Charles H. Small, *EDN,* 4/28/94, p. 55, 8 pp.

Reconfiguring fault-tolerant two-dimensional array architectures. This three-level hierarchy of reconfiguration provides fault tolerance without requiring unreasonable complexity. Nathaniel J. Davis IV, F. Gail Gray, Virginia Polytechnic Institute, et al; *IEEE Micro,* 4/94, p. 60, 9 pp.

Combining microcontroller units and PLDs for best system design. Comparing the performance of Motorola's TPU (time-processing unit) with PLDs shows that a combination is sometimes the most efficient design. Alan E. Clapp, Marquette Electronics, Thomas L. Harman, University of Houston, et al; *IEEE Micro,* 4/94, p. 70, 9 pp.

P-DMOSFET and TSSOP turns on with 2.7 VGS. DMOSFET technology brings lower on-resistance to efficiently manage power for low-voltage systems. Frank Goodenough, *Electronic Design,* 5/2/94, p. 89, 5 pp.

RTOS vendors trade off portability for performance benefits of CPU-specific enhancements. As modern embedded processors gain MMUs and other hardware enhancements, programmers must decide whether or not to use them. Russ Lindgren, *Personal Engineering,* 4/94, p. 31, 6 pp.

