Most Significant Bits

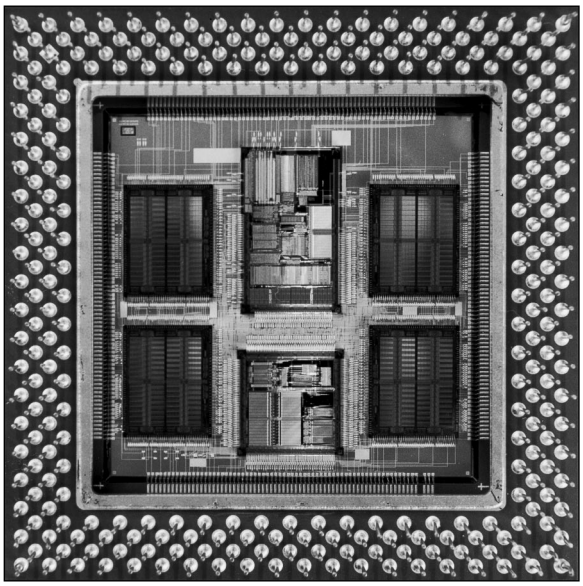
HyperSparc Hits 100 MHz

Taking advantage of its new fab options as a Fujitsu subsidiary, Ross Technology has ported its HyperSparc processor to Fujitsu's 0.5-micron CS-50 process *(see **080504.PDF**)*, boosting the clock speed to 100 MHz and beyond. The original version of HyperSparc, built in a 0.65-micron process by previous owner Cypress, tops out at 66 MHz *(see **071502.PDF**)*. The new version is rated at 111 SPECint92 and 135 SPECfp92, about 25% faster than the top-of-the-line 60-MHz SuperSparc.

The new HyperSparc, available in 80- and 90-MHz versions as well, is packaged in a 131-pin multichip module, as the photo below shows. This module combines the two-chip processor with 128K or 256K of cache memory. Only a single bus, the 64-bit MBus, leaves the module, resulting in the low pin count.

Ross will market the new HyperSparc to OEMs in the MCM as well as mounted on standard MBus boards containing one or two processors. These boards are compatible with the large installed base of MBus SPARC systems at bus speeds up to 50 MHz; the boards contain a voltage converter to generate the 3.3-V power used by the 0.5-micron processor. As it did with the original HyperSparc, Ross will also supply MBus boards as end-user upgrades.

Along with improving performance, the new process should reduce cost as well. The new CPU chip measures 135 mm^2, while the cache-management chip is now 90 mm^2. The MPR Cost Model *(see **071004.PDF**)* estimates that the two-chip set costs about $140 to build, a 10% reduction from the 0.65-micron version. The cost reduction would be greater except for the cost of the MCM package. This package, however, greatly reduces the processor footprint and thus PC board costs.



The new HyperSparc module contains the CPU (center top), cache-management chip (center bottom), and four SRAM chips in a single 131-pin ceramic PGA package measuring 45 × 45 mm.

It isn't clear that this manufacturing cost advantage will turn into a price advantage, as Ross did not announce volume pricing for the new processor. We expect that the 80-MHz version will sell for around $1,500 in OEM quantities, delivering the same performance as a 60-MHz SuperSparc module for a few hundred dollars less. The 100-MHz version, with better performance, should list for about $2,000. Ross is currently sampling these products to OEMs, with production slated for 3Q94. The company also hopes to sample a 110-MHz version in 3Q94.

The new HyperSparc allows Ross to offer better performance than SuperSparc at a similar price. By the time the new Ross chips are available, however, TI plans to ship SuperSparc-2 chips with better performance; how these chips compare remains to be seen. Sun continues to evaluate HyperSparc but may, as it has in the past, stick with its own SuperSparc design for its systems. If HyperSparc can show a cost advantage over TI's chips, it may find a place in Sun's midrange systems.

Sun Expands Fujitsu Relationship

Seeking to rationalize SPARC processor development, Sun and Fujitsu have agreed to coordinate their efforts and develop a single roadmap for the future. Fujitsu has been a long-time supporter of SPARC, but current subsidiaries Ross Technology and Hal Computer have spent about $100 million developing processors that compete directly with Sun CPU designs (see previous item). Although the agreement will have little effect on processors scheduled for release in the next year, the companies expect to have a single unified roadmap for SPARC processors developed after that time; this roadmap could be made public as early as this summer.

The initial version of the roadmap looks very much like Sun's original three-family plan *(see **070404.PDF**)*: a low-end family, a midrange family based on SPARC v8, and a high-end family based on the new version 9 architecture. These families are currently based on MicroSparc, SuperSparc, and UltraSparc, and this is unlikely to change. The most probable scenario is that there will be no follow-ons to HyperSparc-2, which is planned for 2Q95 at 150 SPECint92, or to Hal's PM-1 processor, now expected to deliver 225 SPECint92 in 1Q95. Instead, these Fujitsu design teams will probably develop follow-ons to the Sun processors.

Texas Instruments, the other major SPARC player, is not likely to be affected by this agreement, as it is a

foundry and not a design house for SPARC. It continues as the foundry for all SuperSparc chips and UltraSparc.

SPARC Technology Business (STB), a new planet in the Sun system, has turned into a black hole, absorbing all SPARC processor designs in the known universe (with the exception of Hyundai's as-yet-unseen Thunder processor). The agreement essentially eliminates the competition that Sun had originally encouraged in the SPARC chip market. Ross, for example, has kept SPARC processor prices low by aggressively pushing HyperSparc, but this competition may not exist in the future.

Sun counters that competitive pressure from other RISCs will keep SPARC prices in check, and that the agreement strengthens SPARC's hand against the true enemy, Intel. Let's hope that central planning works better for Sun and Fujitsu than it did for the Soviet Union.

Intel Cuts Back on DX4, Pushes Pentium-60

Much to the chagrin of system makers planning aggressive rollouts of DX4-100 desktop systems, Intel has been telling its customers to use the DX4 for portable systems only. DX4 chips are currently available mainly in the 25/75-MHz PQFP version; the 33/100-MHz chips in PGAs apparently will have very limited availability.

There is considerable overlap in integer performance between the DX4-100 and the Pentium-60, and for most users, the DX4-100 looks like a good choice. But other companies will have processors for DX4 sockets later this year, so Intel is trying to push the market to Pentium as quickly as possible. Intel is also promoting PCI, which is more prevalent in Pentium systems. A major push for low-end Pentium systems, including aggressive chip pricing and a $150 million marketing campaign, reportedly will begin this summer.

Intel has not publicly announced this shift in strategy; Cyrix, instead, brought it to light. Intel's reticence may be due in part to a possible reduction in short term profits: Pentium is much more expensive to build than the DX4. Cyrix attributes the shift to problems at Intel's new 0.6-micron foundries. Supporting this theory are reports of limited availability of P54C Pentiums.

Intel insists, however, that there are no problems in the 0.6-micron lines, and that the motivation for the new strategy is simply to drive Pentium into the mainstream as rapidly as possible. Intel currently has more total capacity in its 0.8-micron fabs than in its 0.6-micron lines, and the Pentium-60 uses that 0.8-micron capacity while the DX4 does not. But this new positioning was not discussed when the DX4 was introduced just two months ago, and if Intel's plan has always been to aggressively push Pentium, it is not clear why Intel introduced the DX4-100 at all.

The 100-MHz 486 and Pentium processors received many positive comments and made a strong counter to the PowerPC announcements. But the vast majority of the volume this year apparently will remain at more modest 60-, 66-, and 75-MHz clock rates, and 100-MHz processors—either DX4 or Pentium—may be rare.

IMS Demonstrates x86 Emulation Chip

International Meta Systems is currently testing a prototype of its IMS3250 processor, which uses a RISC-like CPU core to emulate a 486 processor *(see **060603.PDF**)*. The tiny startup company claims that its design will achieve about the same performance, clock for clock, as a 486: most x86 instructions are executed in a single cycle in emulation mode. This feat is attained by incorporating the special x86 addressing modes and condition codes in the CPU core, and by implementing a four-stage pipelined x86 instruction decoder in hardware.

The company expects the final version of the 3250 to run at 60 MHz, matching the performance of a 486-SX2, yet it plans to sell the chip for only $80, about half the current price of Intel's SX2. The IMS chip has only 2K of on-chip cache, however, which could hinder its relative performance on some applications. Also, although instruction execution times are comparable to the 486's, the 3250 will have greater branch penalties because of the predecoder. One advantage is that the 3250 has a limited FPU that delivers much better floating-point performance than the SX2, although it is about half the speed of a DX2.

The 3250 does not use a 486-compatible bus interface, requiring a completely new motherboard design for any PC application. The 3250, however, integrates cache and memory controllers, and the company is developing a companion chip, the 3251, that provides standard PC system logic along with serial, parallel, PCMCIA, and SCSI interfaces. IMS says that its two-chip set could be used in a low-cost, low-power PC-compatible system. The company also hopes that the 3250 will be useful for high-end PDAs and other portable devices.

The target price for the two-chip set is $100. IMS hopes to sample a beta version of the chip set in 3Q94, with the final version in production in 1Q95. The company expects to use SGS-Thomson as a foundry but has not yet signed a final production agreement. Although IMS believes that its rather unusual design does not infringe on any Intel patents, it is seeking an Intel-licensed foundry in hopes of avoiding a costly lawsuit.

One advantage of the emulation strategy is that some algorithms can take advantage of the underlying RISC engine, which IMS rates at 90 MIPS. The company is developing fast speech-recognition algorithms coded natively for improved performance; it also uses the RISC engine to emulate DSP and peripheral functions. Unfortunately, there are no compilers available for the native instruction set, although the company is negotiating with a third party to develop these tools.

IMS is also in discussions with major CPU vendors

to license its emulation technology, which IMS believes would be applicable for other RISC processors. If the IMS technology meets its promises, it could be coupled with a faster RISC core (Alpha, for example) to deliver outstanding x86 emulation performance along with full RISC compatibility. This would require modifications to the RISC core, however. IBM is already developing a PowerPC processor with similar emulation capabilities.

The current prototype includes 68040 emulation, as IMS originally developed its technology for Apple. That company has now committed to software emulation, however, and IMS will remove the 68040 emulation from the final version. During much of the past year, an unnamed major CPU vendor has funded a portion of the 3250 development, but this relationship has also broken off, leaving the small company to market the chip on its own.

By the time the 3250 reaches the market, however, Intel and other vendors will probably be selling 486SX2-class processors for a similar price, leaving IMS to differentiate only on the basis of its RISC-like core and its limited FPU. Its best strategy may be to license its technology to an established processor vendor.

Compaq Aero Uses 486SXJ

Seeking to reduce its costs, Compaq has become the first U.S. system vendor to adopt Intel's 486SXJ processor. The SXJ, which was announced only in Japan, uses a 16-bit bus (*a la* the 386SX) instead of the 32-bit bus in the standard 486SX. The narrow bus reduces system performance by about 10%, according to Intel. The SXJ is otherwise functionally equivalent to the SX and uses the same PQFP package.

Intel has no plans to announce the 486SXJ in the U.S., although it has been selling it in Japan for about a year. Compaq uses the part in its new Contura Aero subnotebook system, but the PC maker markets its product as a 486SX system, ignoring the performance degradation. Because the SXJ is not a regular product, Intel would not reveal its list price. The CPU vendor says that it will discuss the part with any interested customer.

Intel has been under some pressure in the notebook market from low-cost 486 chips from Cyrix and TI. The 486SLC-33, for example, offers about the same performance as a 486SX-25 but sells for only $45 in 1,000-unit quantities, compared with $77 for the 486SX. The SXJ lets Intel offer a 486 part at a price similar to the SLC's without undercutting its 486SX pricing, enticing big customers like Compaq to stay in the Intel camp. Because the SXJ has the same manufacturing costs as a regular SX, however, Intel prefers to promote the more profitable 486SX for general use.

Another sign of price pressure at the low end: Intel has slashed the price of its 486SX-33 to $85, only $12 more than the 25-MHz version. Just a few months ago *(see **080101.PDF**)*, the company had indicated that the SX-33 would carry a $113 price tag in 2Q94, but with AMD and Cyrix pumping out similar parts, Intel could not sustain a 50% premium over the SX-25.

C-Cube Chip Decodes MPEG-2 and DigiCipher

Taking the next step in video decoding, C-Cube Microsystems (Milpitas, Calif.) has unveiled a chip that decodes a variety of compression standards: MPEG-1, MPEG-2, and General Instruments' proprietary DigiCipher-2 protocol. The CL9100 handles all video decompression tasks, requiring only the addition of 1M or 2M of DRAM, depending on the protocol. A separate chip, the CL9110, demultiplexes the MPEG-2 video and audio streams; a third chip, which can be obtained from a number of vendors, is needed to process the audio data.

Like its MPEG-1 predecessor, the CL450 *(see **060803.PDF**)*, the 9100 is based on a proprietary RISC core and contains several special hardware blocks to accelerate discrete cosine transforms (DCTs), Huffman decoding, and other video-decompression functions. The chip runs at 81 MHz internally and is built in a 0.6-micron CMOS process. It supports a variety of input and output resolutions and frame rates, including NTSC, PAL, and film (24 frames per second). Unlike most MPEG-2 chips, it supports the main profile, including bidirectional "B" frames.

Taking advantage of its status as the major supplier of MPEG-2 encoders *(see **0713MSB.PDF**)*, the company has defined extensions to the video standard using optional data fields. Video encoded by a C-Cube processor and decoded by the 9100 will have superior picture quality, according to the company. Decoders from other vendors will still be able to understand video encoded by C-Cube, but the quality will not be as good.

Although MPEG-2 video encoding will be a niche market for the foreseeable future, the decoder market could take off if digital video becomes popular. With its new decoder, C-Cube is well-positioned to take advantage of growth in this area. Incorporating the DigiCipher protocol ensures the company a design win with General Instruments, the largest maker of cable decoders, and is a good hedge against slow acceptance of MPEG-2 in the consumer market.

C-Cube expects to sample the CL9100 in 2Q94, with the 9110 following in 3Q94. Each chip will be sold for about $35 in high volume.

Errata: Irda Fax Number

In our last issue, we gave an incorrect fax number for the Infrared Data Association. The correct fax number is 510.934.5241. Irda's phone number is 510.943.6546. ♦

