Literature Watch

ASICs

Blending gate arrays with dedicated circuits sweetens ASIC development. The distinction between gate arrays and standard-cell designs has blended to reveal the SFGA (special-function gate array). Richard A. Quinnell, *EDN,* 3/31/94, p. 29, 4 pp.

Buses

PCI: A long and winding road. With backing from most of the major players, PCI appears ready to serve for the next several generations of machines. W. David Gardner, *OEM,* 3/94, p. 64, 6 pp.

Development Tools

Logic analyzers take on system integration and analysis tasks. Today's logic analyzers are geared toward integrated systems in which bugs can be found only by tracing software. Tom Williams, *Computer Design,* 3/28/94, p. 105, 2 pp.

DSPs

DSPs invade computer world! Digital signal processors provide a bridge between the personal computer and a host of communications and media services. David Lieberman, *OEM,* 3/94, p. 37, 6 pp.

Memory

Low-power DRAMs head for mainstream. The ongoing transition to 3.3-V power simplifies DRAM vendors' efforts to introduce 16-Mbit devices. (Includes directory of DRAM devices.) Jeff Child, *Computer Design,* 3/28/94, p. 42, 5 pp.

RISC and Pentium drive demand for SRAMs that are fastest of the fast. The rapid proliferation of high-speed processors pushes workstations to use sub-10-ns SRAMs. (Includes directory of SRAM devices.) Jeff Child, *Computer Design,* 3/28/94, p. 47, 6 pp.

Flash future bright, despite shortage. Driven by high-volume applications such as cellular phones, memory cards, and BIOS storage, demand for flash memory has surpassed expectations. (Includes directory of flash devices.) Jeff Child, *Computer Design,* 3/28/94, p. 56, 7 pp.

Miscellaneous

Lightweight recoverable virtual memory. This portable implementation of virtual memory provides individual control over atomicity, performance, and serializability. M. Satyanarayanan, Henry H. Mashburn, et al, Carnegie Mellon University; *ACM Transactions on Computer Systems,* 2/94, p. 33, 25 pp.

File system development with stackable layers. This modular file system concept allows complex services to be built from independent layers supplied by multiple sources. John S. Heidemann, Gerald J. Popek, UCLA; *ACM Transactions on Computer Systems,* 2/94, p. 58, 31 pp.

EEs in the boardroom. A technical background can help companies make complex decisions and provide a much-needed reality check. Tekla S. Perry, *IEEE Spectrum,* 4/94, p. 20, 5 pp.

Backing up the network. Open networking allows an element of freedom, but backing up a heterogeneous network can be a complex task. Jim Spicer, Mountain Network Solutions; *IEEE Spectrum,* 4/94, p. 66, 3 pp.

Disk arrays. Various combinations of data distribution and redundancy make disk arrays suitable for a broad range of environments. Gregory R. Granger, Bruce L. Worthington, et al, University of Michigan; *IEEE Computer,* 3/94, p. 30, 7 pp.

I/O issues in a multimedia system. With disk-scheduling deadlines set longer than request periods, a multimedia server can support more data streams and efficiently use multiple disks on a SCSI bus. A.L. Narasimha and James C. Wyllie, IBM; *IEEE Computer,* 3/94, p. 69, 6 pp.

A systematic approach to host interface design for high-speed networks. Optimizing software and hardware eliminates system bottlenecks to improve network performance. Peter A. Steenkiste, Carnegie Mellon University; *IEEE Computer,* 3/94, p. 47, 11 pp.

Processors

Designing the TFP microprocessor. Combining mainstream microprocessor technology with supercomputer design techniques helped create a gigaFLOP workstation. Peter Yan-Tek Hsu, Silicon Graphics; *IEEE Micro,* 4/94, p. 23, 11 pp.

Evolution of the PowerPC architecture. Simplifying IBM's POWER architecture enabled the design team to increase clock rates and extend the degree of superscalar operation. Keith Diefendorff, Motorola, Rich Oehler, IBM, et al; *IEEE Micro,* 4/94, p. 34, 16 pp.

Designing, packaging, and testing a 300-MHz, 115-W ECL microprocessor. This full-custom ECL-based microprocessor achieves clock rates triple those of the typical CMOS designs. Norman P. Jouppi, Patrick Boyle, et al, Digital; *IEEE Micro,* 4/94, p. 50, 9 pp.

System Design

A low-cost graphics and multimedia workstation chip set. Three VLSI chips combine to provide a superscalar processor, graphics controller and network, storage, and memory interfaces. Steve Undy, Mick Bass, et al, Hewlett-Packard; *IEEE Micro,* 4/94, p. 10, 13 pp.

