Motorola Fights for Printer Design Wins

Two-Processor 68322 Cuts Cost of 600-dpi Laser Printers

by Linley Gwennap

In an eerie parallel to recent desktop system events, Hewlett-Packard and Apple have been replacing Motorola 68000-family processors with RISC chips to improve the performance of their top laser printers. Although Motorola has given up on the desktop for the 680x0, it is fighting back in the printer market with the 68322.

Over the past year, HP has introduced a line of 600-dpi printers, all based on the i960 processor. Apple favors AMD's 29000 family for its 600-dpi printers. The higher resolution requires four times more performance than 300 dpi, forcing these (and other) companies to move away from the 68000. Motorola has held on to the low end of the market, but 600 dpi is becoming a requirement there as well; BIS Strategic Decisions (Norwell, Mass.), a research firm, projects that sales of 600-dpi printers will exceed those of 300-dpi printers by 1995.

Given this trend, Motorola needed a performance upgrade. The new 68322 combines a 68000 CPU with a graphics coprocessor to efficiently handle 600-dpi images. At $18, the new chip undercuts the price of popular RISC solutions from Intel and AMD and reduces the cost of 600-dpi printers. It is most suited to laser printers that use PCL or Microsoft's new Windows Printing System (WPS), although it can also be used in Postscript printers and even in inkjet printers.

Single Chip Powers Laser Printer

As Figure 1 shows, the 68322 starts with a 68EC000 processor core, which runs at 16 or 20 MHz. The 68000 bus connects the CPU with internal devices and is also brought out to the pins as the host interface. This 16-bit demultiplexed bus supports a variety of common peripheral chips—including Ethernet, Local Talk, and serial interfaces—that can connect the printer to the host system. The chip also includes a bidirectional parallel port, eliminating the need for an external interface chip for this common printer connection.

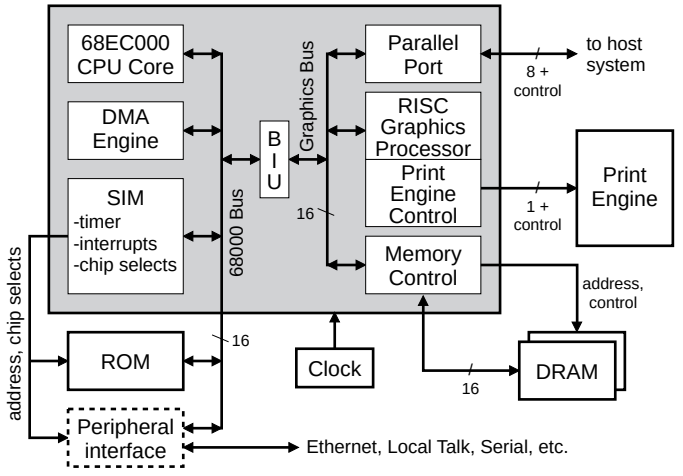

Figure 1. The 68322 combines a 68000 core with a graphics coprocessor and adds system logic for a basic laser printer.

The 68322 includes a DMA engine along with a system interface module (SIM) that contains timers and interrupt logic. The SIM also generates chip selects for external ROM (as in the figure) and other devices. The on-chip DRAM controller supports up to 48M of memory (six banks of 8M each) through a 16-bit bus. Thus, little external logic is needed for most applications.

The other half of the chip is devoted to the graphics coprocessor. This unit connects to the rest of the chip through a 16-bit bus that cycles at the same speed as the 68000 CPU. It contains what Motorola calls the RISC graphics processor (RGP), which is neither RISC nor CISC but instead is a special-purpose processor. This dedicated design reduces complexity and increases performance for its specific task.

The RGP is programmable using 31 instructions, most of which perform bit block transfers (bitBLTs) or decompress run-length-encoded scanlines. These operations occur entirely in memory; the RGP has no general-purpose registers. The instructions use a variable-length encoding of 2 to 28 bytes, reducing code size compared with a fixed-length instruction set. The bitBLT engine performs all 256 Boolean operations on source and destination data with halftone overlays.

The RGP is directly coupled to the print-engine video controller (PEVC), which provides a glueless interface to Canon, Ricoh, and other common laser engines using 10 signal pins. This interface can sustain throughput of 10–15 Mbps, adequate for eight pages per minute at 600-dpi (dots per inch) resolution.

The 68322 is a static design built in 0.8-micron, three-layer-metal CMOS. The CPU core is fully custom, but the remainder of the chip is a standard cell design, reducing development time. Although this approach reduces circuit density, the 308,000-transistor chip uses only about 50 mm^2; thus, there is little reason to further compact the design.

The production version of the 68322 uses a 160-pin PQFP. A development version is also available that uses a 208-pin PGA to bring out additional signals from the CPU core for debugging.

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One issue that the 68322 does not address is image enhancement similar to HP's RET (resolution enhancement technology) or Destiny's EET (edge enhancement technology). Customers that require this feature can add Destiny's EET chip *(see **071001.PDF**)* between the 68322 and the print engine at a cost of $10, approaching the image quality of HP's RET.

Two Processors Work Together

As an image processor, the 68EC000 alone is adequate for most 300-dpi printers but is woefully underpowered compared with the RISC engines in i960 and Am29000 processors. By adding the graphics coprocessor, however, Motorola claims that the 68322 has enough performance for a low-end 600-dpi laser printer.

Motorola designed the chip in conjunction with Peerless Systems (Redondo Beach, Calif.) to take advantage of the two-step processing method used by that company and other printer software vendors. With this method, a typical printer CPU would translate the page-description language (PDL) into an intermediate format called a display list. The display list contains a set of objects instead of a bitmap image of the complete page. These objects are run-length encoded for further compression. This technique can be used with any PDL, including Adobe's Postscript, HP's PCL, and WPS.

Although the display-list method can be (and is) used in single-processor systems, it is ideally suited to a two-processor configuration, as in the 68322. The 68000 builds the display list, which contains the RGP instructions for processing the list along with the objects to be printed. The RGP then executes these instructions to generate an image of the page and sends that information to the print engine using the PEVC. Because the RGP is autonomous, it can process the data for one page while the CPU creates the display list for the next page. Motorola claims that, together, the two processors match the performance of more powerful RISC chips.

In addition to reducing the cost of the processor chip, the display-list algorithm also cuts overall system cost by reducing the memory required. Memory is often the largest cost in a low-end 600-dpi printer; to handle a full page with some buffering, these printers must contain 4M–8M of DRAM. The display list can be scanned quickly to locate items in a particular portion (or band) of the page; that band can be sent to the print engine while the next band is being assembled. With banding, the software never creates an entire rasterized page in memory, reducing the minimum requirement to 512K for PCL or WPS printers or 2M for Postscript.

Existing printer software must be modified to take advantage of the 68322's RGP. Peerless is the only vendor that has committed to this port and plans to offer PCL, WPS, and Postscript emulation. Because Peerless is a licensed Postscript vendor, Motorola does not expect Adobe itself to offer a 68322 version of Postscript. Other software vendors, such as Destiny and Phoenix, are evaluating the 68322 but have made no public commitments.

Price and Availability

The 16-MHz 68322 is currently sampling; Motorola expects to begin volume shipments of 16- and 20-MHz parts later this month. In a 160-pin PQFP, the 16-MHz chip is priced at $17.95 while the 20-MHz version sells for $21.54, both in quantities of 10,000. For more information, contact your local Motorola sales office or call Mike Frawley at 512.891.2154.

Cutting Prices to a New Low

The 68322, with its graphics coprocessor, allows Motorola to play in the 600-dpi market. A low-cost 600-dpi printer with a parallel port can be built from the diagram in Figure 1 using only a 68322, clock chip, ROM (for built-in fonts and the control code), at least 512K of DRAM, and a print engine. For a small incremental cost, a Local Talk or Ethernet interface can be added. BIS estimates that this design could be sold for less than $500, comparable to the price of some inkjet printers.

A similar product based on the i960 would use an i960KA processor instead of the 68322. The Intel chip does not have integrated peripherals, however. To solve this problem, Intel has developed the i961KD printer coprocessor chip, which integrates most of the remaining functions of the 68322 and, like the Motorola chip, includes an autonomous coprocessor. The KD does not have a built-in host interface, so a third chip must be added to provide a parallel, serial, or other interface.

In 10,000-unit volumes, the 16-MHz KA/KD combination sells for $52, plus another few bucks for the serial or parallel interface. This more expensive solution offers better performance—faster printing and/or higher resolution—than the 68322. Replacing the KD with Destiny's 8905 *(see **071001.PDF**)* places the combined cost at $39 but eliminates the coprocessor and reduces performance. The 68322, in contrast, sells for $18. This price gap should get the attention of many vendors.

AMD offers the 29205 as a single-chip printer solution. This chip integrates all required system logic, a print-engine interface, and serial and parallel ports to connect to the host system. At 16 MHz, the chip has enough power for a low-end 600-dpi printer but costs $29 in 1,000-unit volumes, still significantly more than the Motorola chip.

Unless Intel and AMD adjust their prices, the 68322 should prove attractive to many laser-printer vendors. HP, the biggest of all, has historically used customized system-logic solutions, but the 68322 is a good fit for many second- and third-tier printer vendors. ♦

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