Most Significant Bits

Digital Announces World's Fastest CPUs

Jealously guarding its role as the vendor of the world's fastest microprocessors, Digital announced new software and hardware enhancements that allow it to retain a lead in integer performance over the recently announced Power2 from IBM *(see **071301.PDF**)* and all other microprocessors announced to date. The new software includes compiler and operating system enhancements that boost the 200-MHz 21064, coupled with a fast 4M of cache, to 132.7 SPECint92 and 200.1 SPECfp92. These new figures provide a 5% lead in integer performance over the IBM processor, but lag by 30% on floating-point. The new software is available immediately.

To bolster its lead, Digital announced at the Microprocessor Forum that it has developed a new processor, unimaginatively dubbed the 21064A, that uses a 0.5-micron CMOS process to raise its clock frequency as high as 275 MHz. The 21064A processor core is similar to the current 21064, but since a simple shrink of the 21064 would have resulted in a pad-limited die, both the instruction and data caches have been doubled in size to 16K each, using up the extra die area. The larger caches allow the new chip's performance to scale more linearly with clock frequency, even at such eye-popping speeds.

Along with the larger caches, the 21064A has a few minor enhancements to improve performance. The branch history table has been expanded from one to two history bits, using a two-bit prediction algorithm similar to that of Pentium *(see **070402.PDF**)*. Digital believes that the new algorithm will improve prediction accuracy by 5–10%. The 21064A also has a new FP divider that retires two bits per cycle using a variable-length algorithm that is twice as fast as the 21064's divider.

With the new process, the die area is 164 mm^2, 15% smaller than the 0.6-micron 21064. A fourth metal layer helps compact the design, but the pad ring prevents the die area from taking full advantage of the new process. Despite the higher wafer cost and high initial defect density of the new process, the MPR Cost Model *(see **071004.PDF**)* indicates that the smaller die will reduce manufacturing cost by about 10% from the 21064, to around $190.

Digital has chosen to reveal its new design well in advance of actual shipments. The initial speed grade of the 21064A will be 225-MHz; the company expects to sample this version in December but will not be in production until next July. The 275-MHz part is planned to sample in 1Q94 and reach production in 3Q94.

As the new high end of its Alpha line, the 21064A will bear a premium price: $965 for the 225-MHz version and $1586 for the 275-MHz part, both in 1K quantities. The slower version is priced comparably to current high-end R4400, SuperSPARC, and Pentium chips. The high-speed part carries a significant premium but bears a comparable dollars/SPECint92 ratio. IBM's Power2 chip set is not sold on the open market; if it were, its multichip design might necessitate an even higher price than Digital's already steep prices.

Digital's Kevin Fielding estimates that the new chip will reach 170 SPECint92 and 290 SPECfp92 in a high-end configuration with 4M of 10-ns SRAM. These figures are based on simulations; the company has only recently received first silicon of the 21064A. If Digital's estimates are accurate, the 275-MHz 21064A will surpass Power2 in both integer and floating-point, although IBM may improve its ratings by the time the 21064A begins shipping. No other vendor has yet announced a microprocessor with performance greater than 100 SPECint92.

Digital's revelation helps neutralize the publicity garnered by IBM's Power2 announcement. It also shows that, despite the tremendous clock speeds of its current Alpha processors, they will continue to get faster as circuit technology improves. Finally, the pricing of the new parts, which is effective in 3Q94, implies that the 200-MHz 21064, currently priced at $1304, will drop to below $800 by next summer.

NexGen Quietly Samples 586, At Last

Sources in Taiwan report that samples of NexGen Microsystems' "586" microprocessor have been delivered to several computer makers there, although the company itself refuses to comment. The two-chip set includes an integer unit and an optional math coprocessor chip. NexGen has spent more than six years and approximately $100 million developing its x86-compatible processor, which has been through several redesigns. It started as an eight-chip design and only recently was compacted to put the entire integer unit on one chip. Like Cyrix's M1 design *(see **071401.PDF**)*, the NexGen processor has a more aggressive microarchitecture than Pentium, with register renaming, speculative execution, and out-of-order execution, so it should be faster at the same clock rate; the trick will be matching Intel's clock speeds.

All these years of development reportedly have enabled NexGen to work the bugs out of its design. The new two-chip implementation uses the same logic as the earlier multichip design; as a result, NexGen claims the design is relatively bug-free. The initial silicon is believed to have been fabricated by Hewlett-Packard, whose Intel patent license should make a legal challenge difficult—unless the US Supreme Court overturns the lower-court rulings that endorsed this foundry-licensing strategy. Since HP is getting out of the foundry business, however, NexGen will have to find another Intel-licensed foundry.

NexGen's two-chip processor may be faster than Intel's Pentium, but for Taiwanese computer makers, it has an even more important advantage: availability. Only the largest Taiwanese companies have seen Pentium samples; based on their experience with the 386 and 486, most computer and motherboard makers there expect to have difficulty getting volumes of Pentium chips. Even if they do obtain the chips, they don't expect to get prices comparable to the large US system makers. This situation has left them eager to do business with Intel's competitors, a fact that AMD and Cyrix have already exploited quite successfully.

Orion Announced as R4600

At the Microprocessor Forum, IDT and Toshiba jointly announced availability of the R4600, previously known as Orion *(see **061507.PDF**)*. The new MIPS-architecture processor is a low-cost design with Pentium-class performance. It is faster than the R4200 *(see **070701.PDF**)* but significantly more expensive. Both new MIPS chips, however, are much less costly than Pentium. The R4600 should be particularly attractive to NT system vendors.

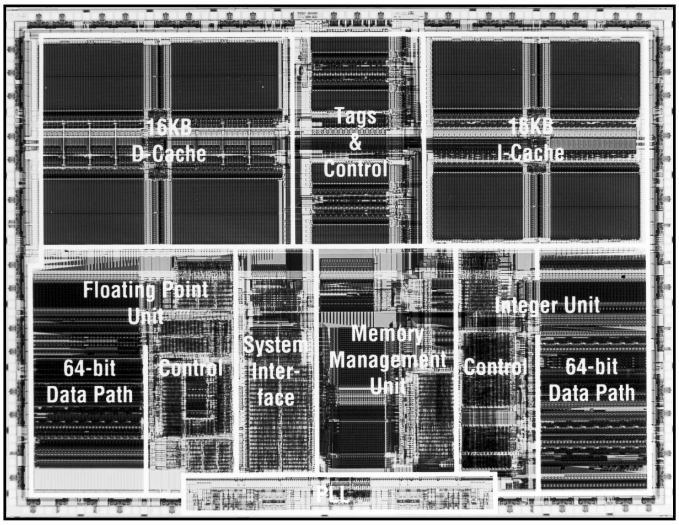
IDT expects to sample the R4600 in 4Q93 with volume production in 1Q94. The initial version will have a clock rate of 100 MHz (internal) and will operate at 5 V. IDT's initial price for 10K quantities is $240, which the company expects to drop well below $200 by the end of 1994. Lower-speed versions in a plastic package may be offered below $100 at that time.

Toshiba will focus initially on 3.3-V versions of the R4600. The company plans to sample 100-MHz parts at this voltage in 2Q94 with production the following quarter. Volume pricing for the low-voltage parts will be $250, slightly higher than IDT's price.

The new processor is compatible with Toshiba's Tigershark chip set *(see **0709MSB.PDF**)*, which converts the R4x00 system bus to a 486 bus, allowing the R4600 to be used with standard PC system-logic chips. Toshiba is rumored to be developing an R4x00-to-PCI bridge as well. The R4600 is also supported by DeskStation's new MipsCore chip set (see next item).

The low pricing is made possible by the R4600's small die size. The design, done by QED (San Jose, Calif.), fits on a die just 77 mm^2 using 0.64-micron, three-layer-metal CMOS. This is slightly smaller than either a 0.8-micron 486DX, an R4200, or a PowerPC 603 *(see **071402.PDF**)*. The MPR Cost Model *(see **071004.PDF**)* estimates that the manufacturing cost of the R4600 is about $55, around 40% more than either the 486DX or the R4200--due to a higher wafer cost and a more expensive ceramic package--but 30% less than the PPC 603.

Unfortunately, the companies have not made much progress in verifying the performance of the new chip. The initial parts did not function well enough to benchmark; new parts are being evaluated. The vendors are



Die photo of IDT's R4600, which uses 1.9 million transistors (494K for logic, plus 16 Kbytes of cache) on a 10 × 7.6 mm die.

sticking with earlier claims that performance at 100 MHz will exceed 68 SPECint92 and 60 SPECfp92, based on simulations done by QED. Earl Killian, who presented the information at the conference, expects that the actual chip will do better than these figures and also believes the chip will ultimately run significantly faster than 100 MHz.

WIth the current performance estimates and price, the R4600 stacks up well against Pentium, offering better performance at a third of the cost. The MIPS partners are still working on recruiting the system and software vendors needed to make NT-on-MIPS a viable business.

DeskStation Launches MIPS Chip Set

From deep in the heart of the Silicon Plains (Lenexa, Kansas), DeskStation has disclosed its first chip product, the MipsCore system-logic chip set. The three-chip set is an extension of DeskStation's original system-logic design *(see **070501.PDF**)* that was licensed by IDT but never marketed. That chip set is currently used in DeskStation's line of MIPS-based Windows NT systems.

The new chip set supports all members of the R4x00 processor family, including the new R4600, with external clock rates of up to 75 MHz. The set includes a cache-controller chip, a memory-controller chip, and a bus-interface chip. It supports 512K to 2M of cache and 16M to 256M of system memory using standard SIMMs. The bus interface produces a 486 processor bus that can be connected to local-bus devices or, though standard PC bridge chips, to ISA, EISA, or PCI peripherals.

By coupling the CPU, cache, and memory through a custom, high-bandwidth bus rather than the slower 486 bus, Deskstation expects that its chip set will deliver much better performance than Toshiba's Tigershark, which relies on PC chip sets for memory control. DeskStation intends to announce the new chip set in Novem-

ber, and expects the volume pricing to be less than $100. While this price could be a better deal than a Tigershark/PC-chip-set combination, it is still nearly twice the cost of an equivalent Pentium chip set.

The startup company points out that the three-chip design allows for future derivative products. Swapping the bus chip, for example, could allow a direct interface to PCI. Since only one of the three chips connects to the CPU, another future possibility is support for Alpha, PowerPC, or even Pentium. DeskStation is positioning itself to succeed as a company regardless of which processors dominate the market for NT systems.

Intel Makes Major Pricing Cuts

In releasing its 4Q93 1,000-piece list pricing, Intel has slashed prices on several of its CPUs, including the 33-MHz 486SX and the 50-MHz 486DX2. Large price cuts were also made for most of Intel's 386SX and 386DX processors. Unlike Q3, when most price cuts were limited to 2–3% to offset the increased value of the SL-enhanced parts *(see **070801.PDF**)*, the Q4 pricing includes significant cuts in most product lines except the bread-and-butter 486DX-33, the 486SL (which has been de-emphasized), and Pentium, for which supply still does not meet demand. Intel also revealed a new speed grade, a 3.3-V 486DX2-50. The table at right details the price changes.

Intel Processor	3Q93	4Q93	Decline	Average
i386SX-16p	$35	$33	5.7%	12.0%
i386SX-20p/25p	$49	$42	14.3%	
i386SX-33p	$51	$44	13.7%	
i386DX-16–33p	$82	$72	12.2%	11.9%
i386DX-16–33	$87	$77	11.5%	
i386SL-16nv/20n	$38	$36	5.3%	6.7%
i386SL-20nv	$47	$43	8.5%	
i386SL-20/25n	$47	$43	8.5%	
i386SL-20v/25	$57	$54	5.3%	
i486SL-25	$190	$190	0.0%	1.7%
i486SL-33	$301	$291	3.3%	
i486SX-16–25p	$87	$81	6.9%	12.5%
i486SX-16–25	$92	$85	7.6%	
i486SX-16–25v	$113	$87	23.0%	
i486SX-33p	$163	$121	25.8%	25.8%
i486SX-33v	$171	$133	22.2%	
i486SX-33	$188	$133	29.3%	
i486DX-33/33p	$294	$283	3.7%	3.4%
i486DX-33v	$324	$313	3.4%	
i486DX-50	$444	$432	2.7%	
i486DX2-40v/50	$395	$311	21.3%	16.7%
i486DX2-50v	n/a	$463	n/a	
i486DX2-66	$501	$463	7.6%	
Pentium/60	$843	$818	3.0%	3.0%
Pentium/66	$926	$898	3.0%	

Note: p=plastic package n=no cache v=low voltage (3.3 V)

Hitachi Outlines Roadmap for SH7000

Hitachi's Paul Freet, speaking at the Microprocessor Forum, described four generations of chips based on the SH7000 architecture *(see **071103.PDF**)*. The SH-1 generation includes the SH7032 and 7034, which were announced earlier this year *(see **070802.PDF**)*. These parts, according to Freet, are primarily intended for embedded control applications and PDAs.

At the initial SH7000 announcement, there was some confusion regarding the role of these first-generation chips in PDAs. The 703x chips do not include an MMU, which is required for all announced PDA operating systems. Freet clarified that the SH-1 parts are intended only for fixed-function PDAs, such as the Sharp Wizard, not for general-purpose systems.

The second-generation SH-2 parts are due next year. These parts are expected to deliver 60% better performance based on a higher clock rate and a 4K on-chip cache. (The 7032 has 8K of on-chip memory which is configured as RAM, not cache.) Some new instructions will be added to improve branching and allow for a 32×32-bit on-chip multiplier.

Despite the higher performance, Hitachi intends to maintain the same power consumption as the SH-1 chips. The company also plans to add a phase-locked loop circuit to the second-generation parts to assist in power management. Freet believes that the SH-2 chips will be suitable for high-performance embedded applications, such as networking and laser printers.

The SH-3 parts, planned for 1995, are expected to compete for general-purpose PDA applications. These chips will integrate an MMU and typical PDA peripheral interfaces using 0.5-micron CMOS technology. The goal for these chips is an impressive 90 MIPS at 3.3 V and less than 1 W. A fourth-generation processor with a superscalar core is planned to hit 200 MIPS by 1996.

While each of these generations, taken individually, seems ambitious but achievable, three complete design teams will probably be needed to roll them out on a yearly basis. For Hitachi to publicize such a schedule, the company must have committed significant resources to this program. As many other processor vendors have recently done, Hitachi is disclosing its long-term roadmap to raise the visibility of its new architecture.

If the SH-3 chip meets its goals, it could pack Pentium performance into a PDA form factor. Such a device could solve many of the problems nagging today's first generation PDAs, such as poor handwriting recognition and sluggish response. No vendor other than Hitachi has discussed or even hinted at the ability to develop such a fast, low-power device by 1995, although a power-reduced version of the PowerPC 603 could come close. The SH-3 represents a quantum leap for Hitachi, and it remains to be seen whether the company will be able to bridge that gap. ♦

