Most Significant Bits

SuperSPARC Leaps to 60 MHz; TI Cuts Price

In an effort to match the price/performance of other RISC processors, Texas Instruments (TI) launched a strong one-two punch, announcing another increase in the peak performance of SuperSPARC+ (SS+) while simultaneously cutting the price of the current versions.

At the high end, the company is now sampling SS+ at 60 MHz, a 20% jump from the parts announced just a few months ago *(see **0706MSB.PDF**)*. Although Sun has not yet announced systems using this part, TI expects performance to exceed 75 SPECint92 and 95 SPECfp92. These figures would put SS+ at about the same level as the 99-MHz PA7100, the 150-MHz R4400, and the 150-MHz Alpha, but still well behind the 200-MHz Alpha processor.

TI tags the new chip at about $1000 in quantities of 1000, plus an additional $400 for the required cache control chip (MCC). The total cost is still higher than the $1120 for the R4400 or $860 for the 150-MHz Alpha chip in similar quantities, and also more than the lower-performing Pentium at $1050 (including cache control). The company says it is currently taking volume orders for the 60-MHz grade for delivery within 13 weeks and is confident that it will avoid the problems that restricted delivery of earlier versions of SuperSPARC.

TI also slashed the price of the 50-MHz version in half from the May announcement and now sells the two-chip set for $1080. The company also renamed the 40-MHz version, which does not require the MCC chip, as "SuperSPARC-LE" (SS-LE) and cut its price to $450 in thousands or just $300 in quantities of 10,000. SS-LE, with no external cache, is rated at about 50 SPECint92. At this price, TI expects SS-LE to appear in high-end embedded applications such as document processing, networking, and industrial automation.

While the new performance levels and extreme price cuts give the SuperSPARC family a much better competitive position, the new prices are still a bit high compared to similar RISC chips. SS-LE is the most compelling, since it achieves its performance without any external cache, stacking up well against the 50-MHz PowerPC 601 and the R4000PC. The new 60-MHz SS+ is in the same performance neighborhood as other popular RISCs and comfortably ahead of Pentium.

AMD Cleans 486 Chips, Adds 486SX

As expected *(see **070601.PDF**)*, AMD announced that it is now using "clean room" microcode in its Am486 processors, eliminating its dependence on Intel microcode. Although the two companies are still adjudicating AMD's right to use the Intel microcode, the move to internally developed microcode reduces AMD's exposure should Intel eventually triumph in court.

The company has also added a 486SX family to its previously-announced 486DX chips. Using the same strategy as for its DX parts, AMD has priced its 486SX-33 at $185 in quantities of 1000, nearly identical to Intel's pricing for the same processor. AMD offers a 40-MHz 486SX for the same price, giving customers a free performance boost not available from Intel. AMD's 486SX is also available in a low-voltage 33-MHz version, also priced at $185. The new SX parts actually use the same die as the DX parts; AMD has not yet redesigned the part to eliminate the floating-point unit.

AMD will offer its DX parts with either Intel microcode or AMD microcode during an extended "transition" period, but the SX parts will be sold only with the clean room code. AMD hopes that its SX appeal will incite vendors to take a chance on the new microcode, and eventually will build enough of an installed base to demonstrate full compatibility with Intel's processors, just as Cyrix's processors are now accepted as fully compatible.

Like AMD's first 486 products, the new chips stay well within Intel's pricing umbrella. The only differentiation is the availability of 40-MHz parts, which Intel has so far chosen not to offer. Intel will not feel threatened unless AMD significantly cuts its prices or begins to offer variations—such as higher-frequency SX chips—that would disturb Intel's pricing structure. In the meantime, Intel will continue to scare potential AMD customers with legal issues.

Speaking of legal wrangles, the Court of Appeal denied AMD's Petition for Rehearing that asked the court to reconsider its ruling overturning the award of 386 rights in the AMD/Intel arbitration *(see **0708MSB.PDF**)*. This rejection, which was expected, clears the way for AMD to take its case to the California Supreme Court. (In last issue's news item, we mistakenly said—it was a late night—that the jury had ruled against Intel in the 287 microcode case. In fact, of course, the jury ruled against AMD. In any case, the judge has overturned the jury verdict, and the issue will be retried.)

VLSI Previews x86 PDA Processors

At the MicroSystems Forum, VLSI Technology VP Henry Potts gave the first concrete details on the products that will emerge from its alliance with Intel. The first product, code-named Polar, is a two-chip set that provides all the functions for a basic handheld device. One chip includes Intel's static 386SX CPU core, SMM, a DRAM controller, and an accelerated LCD-display controller optimized for pen-based systems that could produce 6–10 WinMarks. The second chip has all the I/O peripherals; application-specific customization is expected

to focus on this chip. Samples are promised for the fall. Potts expects volume pricing to be under $50 and power consumption to be under 600 mW for the two-chip set. Polar could be used in products that sell for about $600.

A few months behind Polar, the 486-based Draco chip set will roll out. The two-chip set includes all the same functions as Polar, optimized for higher performance but without the on-chip CPU core; it is designed to work with an "SL-Enhanced" 486 chip. Potts said the Draco chip set, including a separate 486 processor, will cost less than $100. Since the least-expensive 3.3V 486 sells for about $70 today in volume, this implies a chip set price of about $30. Potts expects Draco to be used in $1000 systems.

These chips will be marketed primarily by VLSI Technology, although Intel also has rights to sell them. Intel will fabricate the chip containing the CPU core, and VLSI will fabricate the other chips. Both products are aimed at the "smaller than subnotebook" market.

AMD Pursues Palmtops With Elan

AMD refused to comment on published reports that it, too, will offer a 386-based integrated processor for handheld devices later this year. Code-named "Elan," the new chip combines AMD's static CPU core with an enhanced set of system-logic functions from Taiwanese chip-set vendor Tidalwave. The 208-pin, 3V device is expected to sample in November, with pricing rumored to be approximately $45 in volume. The initial application is likely to be palmtop PCs, with true PDAs coming later.

Elan is a product of the Customer-Specific Products Division that AMD founded last year. Sources indicate that the Elan chip may be more important as a starting point for customer-specific variants than as a standard product. The expectation that these variants would be necessary was also a key reason for Intel's decision to work with VLSI Technology on integrated products.

RISC Vendors Vie Over Future Cable Boxes

A recent flurry of activity makes it seem that interactive digital cable television is not just a string of buzzwords but has become the hottest non-existent market since PDAs. Processors currently vying for a spot on top of the TV of the future include MIPS, PowerPC, and the omnipresent x86. The concept of the digital set-top is a device that can access and decode up to 500 channels, provide two-way communication, and execute video-game and educational software. These abilities could enable video-on-demand, information services, home shopping, and potentially even video conferencing.

Silicon Graphics (SGI) is closest to deploying a prototype, announcing that it has formed a partnership with giant Time Warner Cable to test a MIPS-based product with 4000 customers in Orlando (FL) starting late this year. The box will employ a processor based on an R4000 core and a Toshiba MPEG decoder chip. SGI Challenge systems, with up to 36 processors, will be used as digital video servers in central locations. SGI is developing its own user-interface software for this pilot program.

Motorola has teamed with Scientific Atlanta, a cable box manufacturer, and Kaleida, an Apple spin-off, to promote a PowerPC set-top. The program will combine an embedded derivative of the PowerPC 603 with an MPEG decoder and Kaleida's ScriptX software. Although this group expects to have a prototype system ready by mid-1994, no cable companies have publicly committed to this project.

A third group consists of three industry giants: Intel, Microsoft, and General Instrument (GI), the top manufacturer of cable boxes today. These companies hope to make the TV of the future look like the PC of today, with an x86 processor running a derivative of Microsoft Windows. The projected product will decode either MPEG or DigiCipher (a GI technology) video using a C-Cube/TI chip set. This gang of giants also has no public commitments from cable companies, although GI hopes to exploit its relationship with the nation's largest cable company, TCI Cablevision, to convince it to back the program.

3DO hopes to gain access to the set-top through its next-generation video-game units *(see **0701MSB.PDF**)*. AT&T and Sanyo have joined Panasonic in licensing 3DO's Interactive Multiplayer technology. The 3DO system will use an ARM processor with an optional C-Cube chip for MPEG decoding. AT&T also announced a deal with Sega to produce a system that allows multi-player video games over standard phone lines.

These companies and others are eyeing the 100 million television sets in the US alone as a potential market for futuristic video services. Unlike business customers, however, home users will buy only if the product has a low price, putting the squeeze on hardware vendors to reduce their costs. Another important factor in this market is ease of use; consumers who can't stop the "12:00" from flashing on their VCRs will balk at using a complex user interface just to channel surf. Eventually, your television may provide a multimedia window on the world, but there will be many false starts before that comes to pass.

Data General Rescues 88110 From Oblivion

Despite our pessimistic comments last issue, Data General (DG) announced a family of new Aviion systems based on Motorola's 88110 processor. DG decided to stick with the 88000 architecture to maintain compatibility with its installed base of 20,000 Aviion systems, a number slightly less than Sun's monthly SPARC shipments. The new products range from the $15,000 AV500 workstation to the $280,000, 16-processor AV9500 server.

The new systems, which are shipping today, use 40-MHz and 45-MHz versions of the 88110. Motorola ad-

mits that it still has not reached its target frequency of 50 MHz for the complex speculative-execution processor (see µPR 12/4/91, p. 1) and now claims that 50-MHz parts will be available "later this year." DG is not so sure; its announcement included a few 50-MHz systems that it expects to ship by 2Q94.

Data General rates its 45-MHz systems at 45 SPECint92 and 47 SPECfp92. These are the first measured SPECmark ratings for the 88110, since the only previously announced design wins were for Harris' real-time systems and an IBM X-terminal.

These ratings (assuming that they scale to 50 MHz) are at the low end of Motorola's initial projections, and are significantly worse considering that Motorola's projections were for a cacheless system while the DG boxes include a 256K external cache. The interminable delays and significant reduction in performance could indicate problems with such aggressive superscalar techniques.

IBM RSC Hits 45 MHz

IBM announced that its new RS/6000 Model 230 workstation is based on a 45.5-MHz version of its RSC chip. The 36% increase in speed from the original RSC is due to a process shrink from 1.0 micron to 0.5 micron CMOS. The new chip does not use the five-layer-metal PowerPC process but rather a three-layer-metal process derived from IBM's 16-Mbit DRAM production line. The shrink reduces the die size from about 225 mm^2 to 75 mm^2.

The new version is functionally identical to the original. Although the RSC does not directly control a secondary cache, IBM added a 128K cache to the Model 230 using an external cache controller. This cache and the higher clock rate give the new system ratings of 24 SPECint92 and 40 SPECfp92, matching the performance of microSPARC-based systems. The faster RSC should satisfy the low end of the RS/6000 line until PowerPC 601 systems begin shipping late this year. If the 601 should falter, it seems likely that the new process would support a faster RSC.

LSI Upgrades 33020 X-Terminal Controller

LSI Logic announced the LR33120 processor for X-terminal applications, offering 25% more performance than its predecessor, the 33020 (see µPR 10/30/91, p. 8). It achieves this increase through two significant enhancements. The new chip adds support for fast-page-mode DRAMs and doubles the size of the source queue in the graphics unit. LSI claims to have the industry's fastest X-terminal chip, with a rating of over 150K Xstones at 40 MHz, but the 33120 will not begin sampling until 4Q93 and even then will be available only at 25 and 33 MHz.

Like the 33020, the new chip combines a MIPS R3000 core with a BitBLT engine, video controller, and other I/O functions generally used in X-terminals. The 33120 will use a 208-pin metal QFP compatible with the '020. The new chip is slated for volume production in 1Q94 at $70 for the 25-MHz version and $85 for the 33-MHz version, both in quantities of 10,000.

R4000 Chip Set Slips Into 1994

Toshiba announced scheduled availability for the MIPS-designed R4000-to-486 chip set *(see **070501.PDF**)* that it is now calling Tigershark. Although MIPS had aggressively planned for sampling in 2Q93, Toshiba is now quoting 4Q93 for samples and 1Q94 for volume production. MIPS had also hoped that pricing would be under $30, but Toshiba says that 1000-piece pricing will be less than $65 for the two-chip set.

Toshiba also revealed that the initial design will support both 5V and 3.3V processors, the latter being necessary for the 150-MHz R4400 and for the R4200. The two chips will use 160-pin PQFPs.

With the six-month delay, and with IDT still not committed to marketing the DeskStation chip set, it seems that Acer's PICA chip set will have the low end of market to itself for the remainder of the year. Since the NT-on-MIPS market has yet to take off, the delay will prevent too many players from competing for too few opportunities.

OmniBook, Zoomer Processor Wins Revealed

Hewlett-Packard jumped into the subnotebook market with its OmniBook, a three-pound system based on AMD's 20-MHz 386SXLV processor, a 3.3V version of the Am386SX. The $1515 OmniBook has Microsoft Windows and popular applications software stored in ROM and uses self-refreshing DRAMs for data storage, eliminating the need for a hard drive. Large files can be kept on optional flash memory cards or a removable hard disk, both of which plug into PCMCIA slots. HP claims that, with flash memory, the OmniBook can run for 10 hours on two AA batteries. The 11" × 6.5" system features a pop-out mouse on a stick.

Another portable system, the Zoomer from Casio, rejected all of the current PDA processor options. Instead, it relies on an internally developed CPU based on an NEC V-series core. The 8088-compatible chip runs at just 7 MHz but includes most of the memory, bus, and I/O functions required for the entire system. The $900 Zoomer runs GeoWorks' Geos operating system and uses PCMCIA flash memory cards for storage.

The OmniBook win could be a big one for AMD. Although this is HP's first subnotebook system, the company has had a big success in the palmtop market with its 95LX. The OmniBook is the first system with Windows in ROM, which greatly reduces power requirements, and is pioneering the use of flash memory cards. Casio's Zoomer is less compelling but is one of the first highly-touted PDAs to actually reach the market.

Cyrix IPO Reveals Fab Issues

The prospectus for Cyrix's initial public offering reveals an increasingly contentious relationship with Texas Instruments (TI), one of Cyrix's foundries, driving the company into a closer partnership with its other foundry, SGS-Thomson. While TI's agreement to market Cyrix's 486 designs *(see **060801.PDF**)* was invaluable for establishing the credibility of the smaller company, it left the partners competing for the same customers with the same chips—no doubt the source of much of the conflict.

At this point, the two companies disagree over many aspects of their agreement, although the prospectus does not detail these disputes. The companies are negotiating to resolve their differences, but TI has allegedly threatened to sue Cyrix if these negotiations fail. The situation has gotten so bad that Cyrix now "assumes it will not receive any products from Texas Instruments in the future." According to the prospectus, it is possible that TI could gain a license to all current Cyrix products as well as the next two generations.

Given these circumstances, Cyrix has become more reliant on SGS-Thomson as a foundry, but SGS also holds an option to sell Cyrix processors under its own label. This option is for limited volumes, however, and expires at the end of 1994. To avoid falling into the same competitive situation as it did with TI, Cyrix is negotiating a closer relationship with its European partner that could include the startup taking a minority stake in one of SGS-Thomson's fabrication facilities.

The prospectus also details Cyrix's financial background for the first time. The company's first sales were in 1990, when it sold $25 million of math coprocessors with an incredible 40% net profit margin. This profit was funneled into microprocessor development, and the company began shipping its 486SLC just in time to make up for the collapse of coprocessor prices. The company's sales were about $73 million in 1992 and are growing at about 25% per quarter.

The insecurity of Cyrix's fabless position is clear; the company has no current manufacturing agreements beyond 1994. By strengthening its relationship with SGS-Thomson, Cyrix hopes to alleviate some of the limitations of being a fabless semiconductor company. ♦

And the Winner is...

Ralph Gibson, NEC Electronics, was selected randomly among the MicroSystems Forum attendees who returned evaluation forms. He is the winner of a free one-year subscription to our forthcoming newsletter, the MicroSystems Report. All Microprocessor Report subscribers will receive a complimentary copy of the first issue when it debuts in October.

