VLSI Integrates 486SL Power Management

Other Chip Set Vendors Fight For "SL-Enhanced" Notebooks

By Linley Gwennap

At the recent MicroSystems Forum, VLSI Technology announced new products for notebook computers based on Intel's new "SL-Enhanced" 486 processors *(see **070801.PDF**)*. The "Scamp IV" system-logic chip set is a two-chip set that provides DRAM control along with Intel-compatible peripherals and power management. This chip set connects directly to a special low-cost PCMCIA controller for expansion capability. VLSI ensured its compatibility by licensing technology from Intel.

VLSI's Bert McComas claims that Scamp IV offers the most aggressive power management of any chip set designed for the new Intel chips. He also displayed a 4"× 5" board containing a complete notebook motherboard including a 486 CPU, Scamp IV chip set, 8M of memory, a PCMCIA slot, and a graphics accelerator; he said this was the smallest implementation available from any vendor. The design uses two proprietary buses to reduce pin count, and thus the size, of the individual devices.

Scamp IV Overview

As shown in Figure 1, the 82C420 system controller chip implements the standard set of system logic. It connects directly to the 486 local bus, DRAM, and ISA bus. It also contains the equivalent of an 82C206 plus a real-time clock and CPU power management. The '420 does not support a second-level cache, since most notebook designers do not feel that the extra power and board area required are worth the small increase in performance.

The memory controller handles up to 32M of DRAM in one-, two-, and four-bank configurations. With 80-ns page-mode DRAMs, the chip set returns the first data word in four cycles and subsequent words in two cycles (4-2-2-2 pattern) at 33 MHz. The memory controller also supports ROM and flash memory.

The 82C144 peripheral chip integrates the functions of Intel's 486SL companion chip (the 82360SL) *(see **061501.PDF**)* and adds several standard peripheral interfaces, as shown in Figure 1. The parallel port has extended (ECP) bidirectional capabilities, while the serial port can drive an infrared interface using Hewlett-Packard protocols. With a simple RC network, the two PWM outputs can generate voltages for the LCD display's contrast and brightness controls.

The '144 includes an 8051 microcontroller for interfacing to a PS/2-style mouse and to scanned or unscanned keyboards. It can also be used to monitor and control system power levels without intervention from the main CPU. The '144 integrates all of these functions, eliminating the need for an external controller. By integrating the 8051, VLSI also simplifies communication between the microcontroller and the main CPU with built-in "mailbox" registers.

VLSI licensed the 8051 core from Intel, maintaining compatibility with existing notebook firmware. The 8051 core interfaces directly to external ROM and RAM. The 8051 controls several general-purpose I/O signals that can be used for peripheral control.

Scamp IV has integrated level shifters to drive 5V peripherals even when operating internally at 3.3V. Since most notebooks today use a mixed-voltage design,

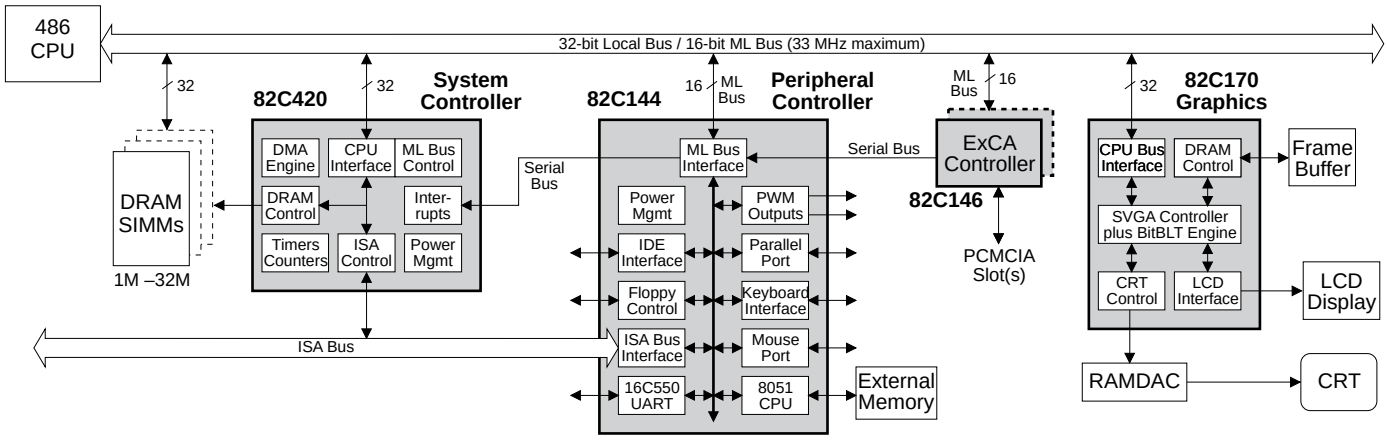


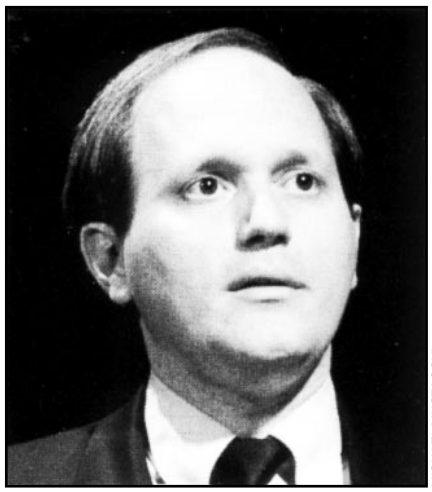
Figure 1. VLSI Technology's notebook chips include the 82C420 System Controller, 82C144 Peripheral Controller, 82C146 PCMCIA Controller, and the 82C170 LCD Graphics Accelerator. VLSI's ML Bus is time-multiplexed onto the low 16 bits of the local bus.

external level-shifting buffers can add significantly to the system cost and board space. VLSI is the only company to announce a chip set with this feature.

Running at 3.3V, Scamp IV works with any 486SX, DX, or DX2 processor with a local-bus frequency of up to 33 MHz. At 5V, it supports a 40-MHz local bus, although Intel does not currently market any CPUs at that speed. (Both AMD and Cyrix sell 40-MHz 486DX chips, but they do not support STPCLK and other Intel features and thus cannot be used with the VLSI chip set.)

New Buses Reduce Pin Count

The chip set uses two innovative techniques to reduce pin count: a 16-bit multiplexed bus and a serial bus. Instead of connecting to the full 32-bit local bus or the complex ISA bus, the '144 communicates to the '420 using what VLSI calls the ML Bus, which uses 16 bits of the 486 address bus as a multiplexed address/data bus. The '420 asserts the 486's AHOLD signal, forcing the CPU to tri-state its address bus, before accessing the ML Bus. Only 21 signals, including a clock, are needed for ML Bus, compared to about 88 for ISA. The ML Bus is clocked at the local-bus frequency, yielding much better bandwidth than the 8-MHz ISA bus.



MICHAEL MUSTACCHI

Bert McComas, of VLSI, announces SCAMP IV chip set at the MicroSystems Forum.

Interrupts and DMA requests are signalled to the '420 via a serial bus, shown in Figure 1. The chip set implements a packet protocol to transfer information across this serial line with minimum latency; the packets are 7 bits long and are clocked at 24 MHz.

Systems with PCMCIA slots can use up to four 82C146 ExCA controllers. Each chip provides all of the configuration and control needed for a single PCMCIA (version 2.0) slot and is compatible with ExCA 1.10 *(see **070103.PDF**)*. It is also register-compatible with Intel's 82365SL controller and requires no external buffers. Both 3.3V and 5V cards are supported.

The ExCA chip uses ML Bus to send and receive data and thus can only be used with the VLSI chip set. It also uses the serial bus to send interrupts for situations such as card insertion. The two low-pin-count buses allow VLSI to use a 100-pin "thin" (TQFP) package with a smaller footprint than any competitive product. At $8.50, the '146 is also the lowest-priced PCMCIA controller yet announced.

Power Management

Scamp IV has extensive support for aggressive power management. It starts with a set of registers that the company claims is "99% compatible" with the 486SL, so existing power-management code can be easily ported. It also includes SMRAM control and other 486SL features required for power management.

VLSI has added several extensions to the basic SL feature set. Any system interrupt (IRQ) can be configured to trigger SMI (system management interrupt). In addition, SMI can be triggered by the internal 8051 or any of the ExCA controllers. Shadow registers maintain the state of write-only peripheral registers so they can be restored after being powered down.

The entire chip set has been carefully designed to eliminate power problems. For instance, if the parallel port is powered down while an attached printer is still turned on, current backdrive can result. Scamp IV places all I/O pins in an appropriate state to eliminate leakage currents without the need for external resistors.

Scamp IV works with both 1× and 2× versions of Intel's enhanced 486 processors. It supports the usual local and global standby, doze, and suspend modes. It also has a unusual 0V suspend mode that disables power to the entire chip set except for a small block of system-monitoring logic.

In addition to the usual clock division, the VLSI design offers "clock division emulation," which toggles the STPCLK signal on and off at a programmable rate to reduce power significantly. In this mode, the processor is always enabled after an interrupt or other system event. The '144 also saves power transparently by shutting down the clock to its internal peripherals when they are not being used.

Notebook Market Heats Up

Although Intel's new processors were announced in June, some vendors are already shipping chip sets that support them, and others have joined VLSI with recent announcements. While ETEQ has aimed its ET8000 *(see **0705MSB.PDF**)* at the "Green PC" market *(see **070905.PDF**)*, other vendors are looking to win notebook designs.

PicoPower was the first to market a chip set compatible with the SL-enhanced processors, announcing its "Evergreen HV" product early this year. The PicoPower chip set uses an external 82C206 to offer the same system functions as VLSI's system controller and does not have a peripheral combo chip similar to the '144. At "about $25," it is priced competitively with the '420 but is available today. PicoPower is already working on a more integrated chip set that it expects will sample shortly after the VLSI chip set.

Price and Availability

The Scamp IV chip set is scheduled to sample in August with volume production in October. The VL82C420, in a 208-pin metric QFP, is priced at $32.50. The VL82C144, also in a 208-pin MQFP, is priced at $25. The VL82C146 PCMCIA controller, in a 100-pin TQFP, costs $8.50, all in volumes of 1000. For more information, write to VLSI Technology Inquiries, VL170, 200 Parkside Drive, San Fernando, CA 91340; or call Bert McComas at 602/752-6352.

The Evergreen HV is currently available at "about $25" in a 208-pin PQFP. Contact PicoPower at 2680 N. First Street, San Jose, CA 95134; 408/954-8880.

The WD8110ZX is currently shipping in a 208-pin MQFP. It is priced at $22 for the 5V version and $28 for the 3V version, both in quantities of 1000. The WD8120 is expected to sample in July with a volume price of about $10. Contact Western Digital at 8105 Irvine Center Drive, Irvine, CA 82718; 714/932-4900.

The HT27, in a 240-pin PQFP, will begin sampling in August at $55 each with production expected in 4Q93. The HT35 companion chip is currently available for $21 in a 144-pin PQFP. LSI expects to offer the two chips as a set for under $60. For more information, contact LSI Logic Literature Distribution, MS D-102, 1551 McCarthy Blvd., Milpitas, CA 95035; 408/433-8000.

The 2046st is priced at $29 in quantities of 1000. It uses a 208-pin PQFP and is currently in production. Contact ACC Micro at 2500 Augustine Drive, Santa Clara, CA 95054; 408/980-0622, fax 408/980-0626.

VLSI's Graphics Gem

The "Ruby" chip, or 82C170, will provide high-performance graphics in a notebook system. It is one of only two notebook chips yet announced that combines a BitBLT engine with a 32-bit local-bus interface. (Western Digital's 90C24 is the other.)

Like most high-end notebook chips, the '170 supports simultaneous display on both an LCD panel and a CRT. The CRT support is useful for presentations or in a docking station. An external RAMDAC is required to support a CRT display. The LCD interface includes two PWM outputs for contrast and brightness control (in addition to the 82C144's PWM outputs).

The VLSI chip supports a wide range of LCD panel options, with up to 64 shades of gray or 256K colors. It allows CRT resolutions of up to 1024 × 768 × 8, more than most notebook graphics controllers. The '170 also implements four small (up to 128 × 128) overlays that can be used as pop-up control panels for system status or power management. It uses a 208-pin metric QFP.

Ruby will match up well against the WD90C24 and other high-performance chips such as Cirrus' GD-6440 *(see **061603.PDF**)* and C&T's 65535. The VLSI chip is slightly less expensive than the others but does not have an integrated RAMDAC, roughly evening out the cost difference. (VLSI says that its follow-on chip will include a RAMDAC.) These other chips are available today, while the VLSI chip is scheduled to sample in September with volume production in November. The '170 is priced at $28.50 in volumes of 1000.

PicoPower products reduce power even when the processor is fully active by clocking only those subsystems that are in use. The ISA bus, keyboard clock, and other subsystems are controlled in this way. Evergreen also uses CPU clock stretching to reduce power without affecting performance, but this feature can only be used with 2× clock CPUs. The PicoPower chip also includes various timers to monitor system activity, which are similar to but not software-compatible with the 486SL.

OPTi is now shipping its SCNB, or single-chip notebook *(see **0704MSB.PDF**)*. This chip integrates most peripherals, including a microcontroller, but requires an external real-time clock and keyboard controller. Its power-management capabilities are similar to the PicoPower chip, and OPTi also charges $25 for the SCNB.

Western Digital recently began shipping its 8110 system controller, which supports standard 386 and 486 processors as well as SL-enhanced CPUs. The 8110 integrates most system-logic functions but relies on a pair of additional chips for a full set of peripherals. WD says its new 8120, which combines these two chips, will begin sampling this month. The 8110 includes system timers and activity monitors for power management.

LSI HT27 Targets Notebooks

The HT27, from LSI Logic's Headland division, was announced at the same time as Intel's new processors. The HT27 is very similar to VLSI's system controller with its integrated DRAM controller and 82C206 functions. LSI also sells the HT35 companion chip, which includes most of the functions in VLSI's peripheral chip except for the floppy interface and the 8051. The LSI chip set does not directly interface to the ISA bus; instead, it provides only the control signals and requires external buffers for address and data.

The HT27 supports all of the new Intel processors and adds support for 486 chips from AMD and Cyrix as well. It allows bus speeds of up to 33 MHz at either 3.3V or 5V. The LSI chip includes a wide range of event monitors and timers for power-management software.

The unique advantage of the HT27 is its two integrated PCMCIA controllers. Like VLSI's external controllers, LSI's are fully compatible with current standards, but they require external buffers for address and data. For systems with two PCMCIA slots, the HT27 could provide a cost advantage over Scamp IV.

ACC Micro provides yet another option with its

2046st. It is distinguished by its support for an external cache, unlike all of the other chip sets discussed here. The direct-mapped cache can be write-back or write-through and up to 2M in size. External tags are needed. This cache will improve performance, although most notebook designs choose to forego it to save power.

The integrated cache controller forces ACC to leave out other key features. Like the HT27, the 2046st requires external buffers to bridge ISA address and data from the local bus. Some peripherals are included in the separate 3221 chip, but additional discrete chips are needed for keyboard control and the real-time clock. ACC also offers its 2026 microcontroller for external power management.

The 2046st includes a set of power-management features similar to the HT27 but, unlike any chip except for Scamp IV, it includes a 0V suspend mode.

Conclusion

By licensing technology from Intel, VLSI can offer a chip set that, when combined with one of the new Intel 486 chips, provides the same features as the 486SL processor and is compatible with power-management and BIOS code written for that CPU. Other products include a similar set of functions but are not software-compatible with the 486SL, requiring system vendors to rewrite their code.

Many other vendors offer products similar to Scamp IV, and some of them (unlike VLSI's chip set) are already shipping. Scamp IV appears to offer a more integrated and compact solution than any of its competitors, particularly in mixed-voltage designs where its integrated buffers are crucial. One possible exception is LSI's HT27, which may have an advantage due to its integrated PCMCIA controllers. All of the vendors are quite competitive on price, so there is little to distinguish these solutions in that area.

The availability of Intel's SL-enhanced processors has added fuel to the fire in the red-hot notebook market. VLSI's Scamp IV is a good solution for designers who want to maintain compatibility with their old 486SL BIOS code. Vendors willing to redo their software may wish to examine other chip sets. PicoPower, OPTi, and Western Digital have reached the market first but will have to move fast to match the level of integration of the new chip sets from LSI and VLSI. ♦

