Motorola Extends 68300 Line for CD-I, PDAs

68349 "Dragon I," Designed for General Magic Communicators

By Michael Slater

Motorola has introduced two new members of its growing 68300 family of integrated processors, each customized for a particular application. The 68341 is designed to provide a low-cost upgrade path for 68000-based CD-I (Compact Disc-Interactive) home entertainment players, while the 68349 was created in collaboration with General Magic Inc. (GMI) for personal communicators based on GMI's Magic Cap operating system *(see **070303.PDF**)*.

Both chips are derivatives of the 68340 and were designed using Motorola's modular design technique, in which standard modules are connected with an intermodule bus. Motorola's ability to quickly produce derivative designs has resulted in a wide variety of 68300-family chips optimized for various application areas.

The Magic Dragon

The 68349, also known as Dragon I, is part of a two-chip set designed in collaboration with General Magic to provide a highly integrated solution for personal communicators. All functions that are unique to the personal-communicator application are contained in the companion chip, called Astro, which will be available only to GMI's licensees; the 68349, which is openly available, is a general-purpose device that should find a range of applications. While details on Astro have not been released, it apparently includes control for the DRAM, LCD, pen interface, and communication functions.

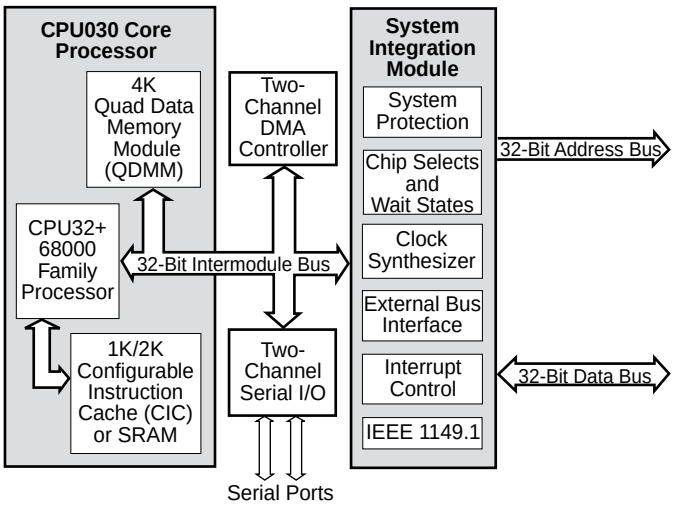

Figure 1. Block diagram of the 68349, which includes a small data RAM and configurable instruction cache/RAM.

The 68349 is the first 68300 family member with an on-chip instruction cache, as Figure 1 shows. The cache boosts performance by providing zero-wait-state operation without requiring fast static RAMs for program memory. The "Configurable Instruction Cache" (CIC) is partitioned into four independent blocks, each of which can be configured as either cache or SRAM. The partitioning can be changed dynamically, allowing the configuration to be optimized for each task.

Each block can provide either 256 bytes of cache or 512 bytes of SRAM; the capacity is larger in SRAM mode because the cache tags become usable for storage. The CIC can therefore provide a total of 1K of cache, 2K of SRAM, or a mix of the two (for example, 512 bytes of cache and 1K of SRAM). The base address for each block configured as SRAM can be set independently.

Each block functions as a separate set when configured as cache. Thus, with all four blocks configured as cache, it is four-way set-associative. At the other extreme, if only one block is configured as cache, it is direct-mapped. Each block can be independently locked, allowing interrupt routines or other critical code to be permanently cached.

The 4K-byte data memory, called the Quad Data Memory Module (QDMM), is also divided into four blocks, each of which has an independent base-address register and write-protection control. Unlike the CIC, the QDMM cannot function as a cache. The QDMM regions are typically used for functions such as scratchpad memory or stacks.

While the CIC and QDMM designations imply that one is for instructions and the other is for data, this distinction is arbitrary; either memory structure can hold instructions or data.

CPU32+ Core

The CPU32+ core in the 68349 is an enhanced version of the CPU32. The CPU32 core has been used in most of the 68300-family chips, including the 68331, 68332, and 68340. This CPU implements a superset of the 68000 instruction set, with most of the 68020 extensions. The principal 68020 capabilities that are not included are memory indirect addressing, bit-field instructions, and coprocessor instructions. It has two instructions not present in the 68020: a table look-up instruction and a low-power stop instruction (see µPR 5/89, p. 1).

The original CPU32 implementation falls short of 68020 or 68030 performance because it has only a 16-bit bus interface and a simpler microarchitecture; for exam-

ple, there is a 4-bit shifter instead of a full barrel shifter, so multi-bit shifts take longer than single-bit shifts. The CPU32+, which first debuted in the 68360 *(see **070603.PDF**)*, extends the data and address paths to 32 bits but does not add any new instructions or provide other enhancements to the microarchitecture. The CPU32+ core has a basic instruction cycle of two clocks (80 ns at 25 MHz).

The CPU32+ core in the 68349 has one new enhancement beyond the 68360: a separate data path between the CPU core and the CIC. This allows instruction fetching to continue while the DMA controller moves data between the QDMM or memory and an I/O device.

Motorola calls the combination of the CPU32+, QDMM, and CIC the CPU030, but this name can be misleading. As noted above, it does not implement the full 68020/030 instruction set, and it also lacks the 68030's MMU.

Figure 2 shows a die photo of the 68349, which is 99.5 mm^2 in 0.8-micron, two-level-metal CMOS, and uses 550,000 transistors.

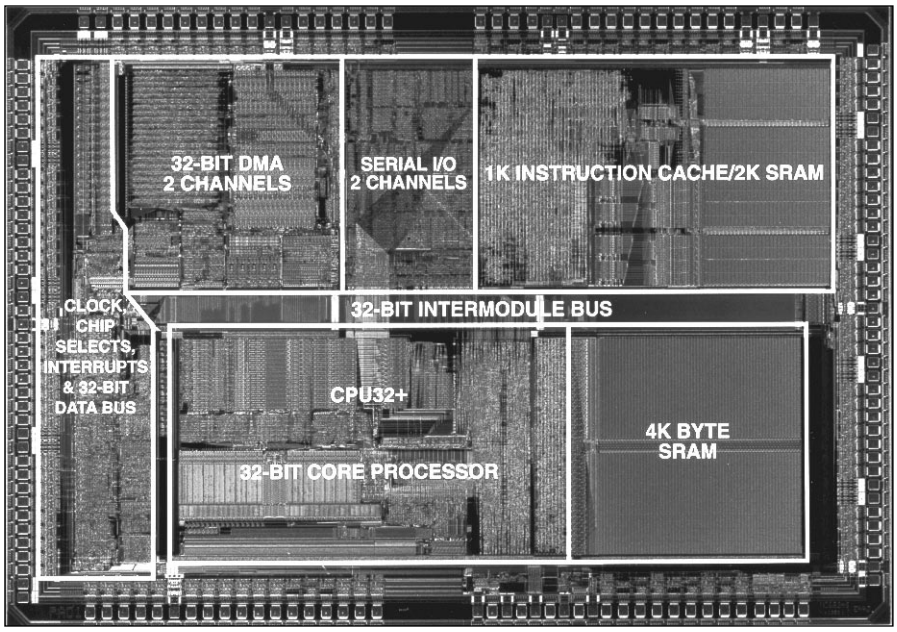

Figure 2. Die photo of the 68349, which incorporates 550,000 transistors on a 11.8 × 8.5 mm (463 × 333 mils) die.

Peripherals

Like the 68340, the 68349 has a two-channel DMA controller. In the '349, the DMA controller has been enhanced to provide full 32-bit addressing. The DMA controller can operate in either single- or dual-address mode with a sustained data rate of up to 50 Mbytes/s at 25 MHz (i.e., one 32-bit transfer every two clock cycles).

The '349 has the same two serial ports as the '340. These ports are software-compatible with the 68681 and are capable of a sustained bandwidth of up to 3 Mbps when operating synchronously. The on-chip baud-rate generator supports asynchronous baud rates up to 76.8 kbps.

The System Integration Module (SIM) in the 68349 provides a full 32-bit bus interface, but it does not include the DRAM control features of the SIM in the 68360 because the Astro companion chip provides memory control. The 32-bit data bus supports dynamic bus sizing for 8- or 16-bit data, simplifying the connection of narrow memories or peripherals. Each of the four chip-select outputs can be independently programmed for base address, number of wait states, and default bus width.

The SIM also includes two 8-bit parallel ports, a bus watchdog timer, a system-protection watchdog timer, a periodic interrupt timer, an interrupt controller with four internal and seven external inputs, and a JTAG boundary-scan interface.

Power Consumption

Since the 68349 is intended for battery-powered personal communicators, power consumption is critical. The chip is available in 5V and 3.3V versions, with a maximum clock rate of 16 MHz at 3.3V and 25 MHz at 5V. At 3.3V and 16 MHz, power consumption is 300 mW. At 5V, power consumption is 640 mW at 16 MHz and 960 mW at 25 MHz. These ratings are what Motorola calls "typical maximum"; they take process variation into account and are measured at the high end of the supply voltage range, but they assume a typical system configuration and instruction mix. Comparing power consumption ratings with those from other vendors is very difficult, because test conditions vary and are often not clearly specified.

The design is fully static, allowing the clock to be slowed or stopped as needed. An on-chip programmable frequency synthesizer allows the clock rate to be slewed over a wide range under software control; with an external 32-kHz crystal, the clock rate can be any multiple of 32 kHz up to the maximum 16- or 25-MHz rate. With the clock stopped, supply current is reduced to 500 µA at 5V, or 315 µA at 3.3V.

A low-power stop (LPSTOP) instruction puts the chip into a standby mode, in which power consumption is reduced to 2.5 mW at 5V, or 1.7 mW at 3.3V. In standby mode, the timers and interrupt control unit continue to operate; the mode is exited when an interrupt occurs. Idle modules can also be individually powered-down under software control.

Upgrading CD-I Systems

While the 68349 is designed to provide higher per-

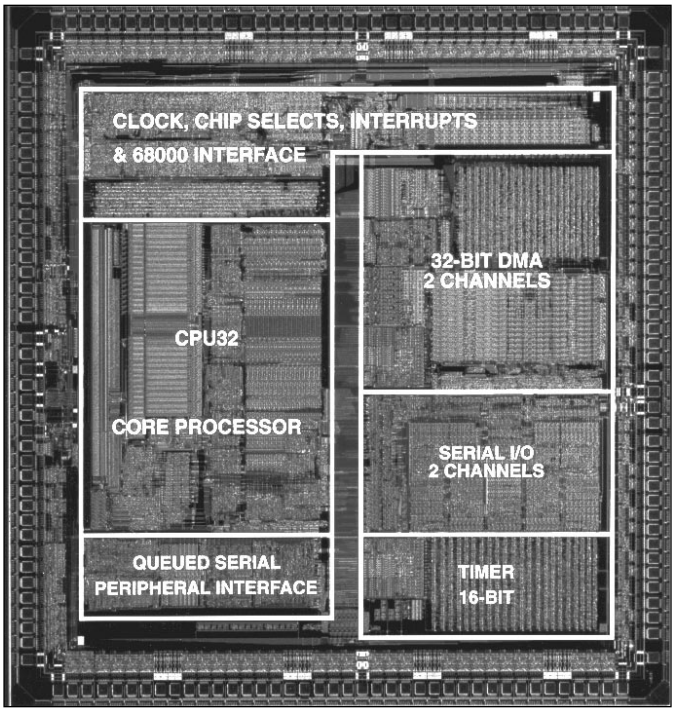

Figure 3. Die photo of the 68341, which incorporates 247,000 transistors on a 9.1 × 8.1 mm (360 × 320 mils) die.

formance than the 68340, the 68341 enables makers of CD-I players to move up from the 68000 at a lower system cost than with the 68340. Motorola had hoped that the 68340 would be used in CD-I players, but makers of these machines have opted for lower-cost implementations based on the 68000 or Philips' 68070 integrated processor. As shown in Figure 3, the 68341 die is 74 mm^2 in a 0.8-micron, two-layer-metal CMOS process.

The 68341, shown in Figure 4, adds a 68000-style bus mode (using the same pins) to the 68030-style bus provided by the 68340. This allows ASICs designed for 68000-based systems to be used with the 68341 without additional glue logic. The 68341 also adds a real-time clock and a Queued Serial Peripheral Interface (QSPI) to eliminate the external chips used for these functions in existing CD-I systems. To trim cost, the '341 eliminates one of the two timers in the '340, since it is not needed for CD-I players. It uses the same CPU32 core as in the '340.

68000 Family Holding Its Own

These two processors illustrate Motorola's ability to adapt its processor designs for specific applications and to work with customers targeting emerging high-volume applications. In the case of the 68349, Motorola's own Paging and Wireless Data Group will be one of the major customers; it plans to introduce a personal communicator based on Magic Cap by the end of this year. By designing the chips for known high-volume applications, Motorola has a relatively assured market for each device. Because they are not really application-specific, however, they will be used in a broader range of applications.

Despite an onslaught of RISC vendors seeking to take away Motorola's embedded processor market, the 68000 family has proven difficult to displace in many applications. Motorola estimates that it will ship about 41 million 68000-family chips in 1993—an order of magnitude more than all RISCs combined.

In many cases, the additional performance offered by RISC processors has simply not been required, and the higher functional integration offered by Motorola's 68300 family has been a major advantage. In the laser printer market, RISC processors are gradually displacing the 68020 and 68030 from performance-oriented segments of the market; HP's LaserJet 4, for example, uses an Intel 960 processor. On the other hand, HP's new low-end printer—the LaserJet 4L—is based on a proprietary, 68000-based integrated processor from Motorola.

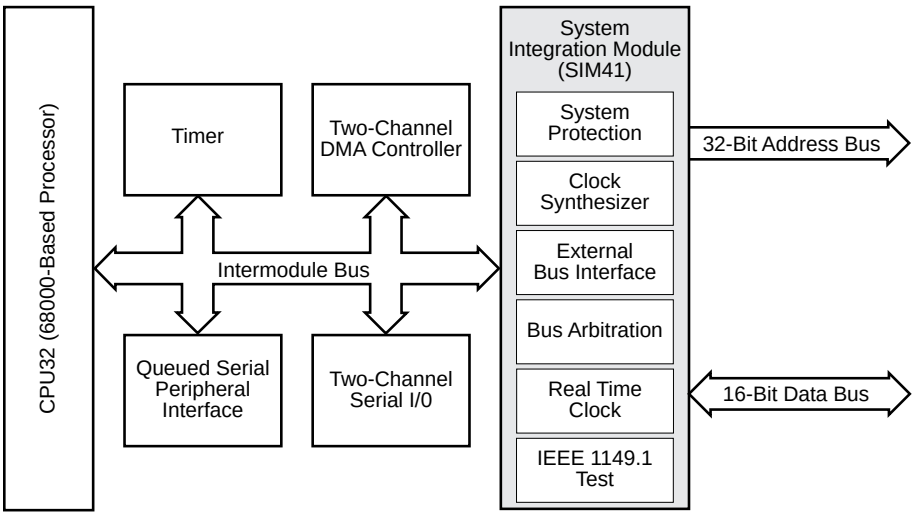

Figure 4. Block diagram of the 68341, which adds a 68000-style bus interface option, a real-time clock, and a serial port to the 68340.

CD-I players represent an enormous potential market, as do personal communicators, but there are significant competitors in both segments. CD-I has been slow to take off, in part because of a limited range of titles and a lack of motion video. Most CD-I titles have been written to support the least-common-denominator of performance among CD-I machines—the 68000—and this has limited what they could do. Motorola hopes that the 68341 will spur a new generation of higher-performance players, which would enable software developers to create applications with more motion and complexity. CD-I could be in for a tough battle against 3DO's Interactive Multiplayers, however, which will

Development Support

Since the 68341 and 68349 are software-compatible with earlier 68300-family processors, a variety of software development tools is already available. In addition, several vendors have announced versions that support the special features of the new chips.

Embedded Support Tools (Canton, MA) has announced a symbolic debugger for the '349 that operates with the on-chip debugging interface, and an in-circuit emulator module that clips on the processor and provides real-time tracing and hardware breakpoints. A version for the '341 will follow. These tools are designed to work with C source-level debuggers from Intermetrics and Microtec Research.

Microware Systems (Des Moines, Iowa) has ported its OS-9 operating system to the 68349, providing direct support for the on-chip instruction cache and DMA controller. Microware also offers a C compiler for OS-9, PC, and UNIX environments.

Price & Availability

Samples of the 68349 and the 3.3V 68349V, as well as the 68341 and 68341V, are available now, with production planned for the fourth quarter. Both devices are packaged in a 160-pin PQFP.

The 5V, 16-MHz 68349 is priced at $28.20, while the 16-MHz 68341 is $21.65, in quantities of 10,000. Pricing for the 25-MHz and 3.3V versions has not been released. The 3.3V 68341V will also be offered in an 8-MHz version.

Contact Tom Starnes at 512/891-2125 or 512/891-2139. For product literature, contact your local Motorola sales office.

debut this fall. The 3DO system uses an ARM processor and a proprietary graphics engine.

Personal Communicator Market Issues

It is not yet clear how much of an issue CPU performance will be for personal communicators based on General Magic's software, since none have yet been publicly demonstrated. That performance is an issue, however, is demonstrated by the addition of the instruction cache in the 68349. Motorola estimates the performance of the 68349 at 8–10 VAX MIPS at 25 MHz (based on Dhrystone 1.1). While accurate performance comparisons are difficult, the 68349 will probably provide about half the performance of either the ARM610 or the Hobbit processors favored by GMI's competitors, or the emerging V810 from NEC and SH7032 from Hitachi *(see **070802.PDF**)*. The RISC chips have a two-to-one advantage in the basic instruction cycle time at the same clock rate, although the difference in average clocks per instruction may not be as great.

On the other hand, the 68349 is both less expensive and more highly integrated than some of its competitors, so the cost of systems based on it could be somewhat lower. The high code density of the 68000 instruction set is also an advantage over ARM, but AT&T's Hobbit, NEC's V810, and Hitachi's SH7000 all claim comparable code density.

In the future, Motorola has several options for enhancing the performance of the 68300 family. A modest speed improvement could be achieved by increasing the clock rate to 33 or 40 MHz, which should be possible if the chips are moved to a more advanced process. More significant, however, are the prospects for entirely new CPU cores. Motorola plans to develop both CPU040 (based on the 68040) and CPU060 (based on the forthcoming 68060) cores for the 68300 line. It is also likely, although Motorola has not publicly committed to doing so, that a PowerPC-based core will be offered.

Motorola has high hopes for the 68349 to be the dominant player in the personal communicator market. Unfortunately, information on the Astro companion chip is not yet available, making it impossible to compare Motorola's system solution to that offered by AT&T. Assuming that the two-chip set provides most of the functions required in a personal communicator, however, it should have an advantage in integration over AT&T's current offerings.

Because so much remains to be revealed—by Motorola/GMI and others—any comparisons of PDA designs today are incomplete. For Newton, no system-logic support chips have been announced, and Intel and VLSI Technology have not yet announced the processor and support chip they are developing for PDAs. NEC and Hitachi have recently joined the competition, and their software alliances have not yet been revealed.

The 68349's success will be determined largely by the market acceptance of GMI's Magic Cap operating system. If customers prefer the Newton software, ARM will profit; and if GO's PenPoint operating system is favored, the battle will be between the x86 and Hobbit architectures. It is also uncertain how soon Motorola will face competition from other architectures running Magic Cap; GMI says that it plans to support other processors eventually, but has offered no specifics.

The personal-communicator/PDA market will have numerous segments, however, and it is possible that most of these architectures will find large markets. It may take many years for volumes to take off, but Motorola is prepared to be patient. Motorola has not given up on Newton either; it is actively campaigning for a second-generation Newton to be based on an integrated Motorola processor, presumably based on a PowerPC core. ♦

