Literature Watch

ASICs

Multilevel ASIC modeling. *Beyond issues of model accuracy and speed, intellectual-property concerns and the lack of standard model formats will force you to mix gate- and higher-level models to simulate complex ASICs.* John C. Napier, Julie Anne Schofield, EDN, 4/29/93, pg 75, 5 pgs.

Denser digital ICs and improved processes unveiled at CICC. *High-performance and more-flexible gate arrays, ASICs, and nonvolatile memories, as well as higher-speed transistors, lead the way.* Dave Bursky, Electronic Design, 5/3/93, pg 43, 4 pgs.

Embedded test bus eases ASIC design and testing. *An on-chip test bus and megacells that pack test logic make it easier to test and emulate ASICs using embedded functions.* Dave Bursky, Electronic Design, 5/3/93, pg 121, 3 pgs.

Buses

Local memory coaxes top speed from SCSI masters. *Increase system throughput by combining SCSI bus mastering with local dedicated memory to maximize data-transfer rates.* Erik Paulsen, NCR; Electronic Design, 4/15/93, pg 75, 7 pgs.

ACCESS.bus. *A new peripheral bus.* Michael Burton, Key Tronic Corporation; Midnight Engineering, May/June, 1993, pg 79, 2 pgs.

Development Tools

Process builds accurate VLSI behavioral models. *New technology uses IC structural data to yield a board-level simulation model by the time a device begins shipping.* Lisa Maliniak, Electronic Design, 5/3/93, pg 63, 5 pgs.

Use Spice to analyze component variations in circuit designs. George Ellis, Kaydon Corporation; EDN, 4/29/93, pg 109, 5 pgs.

DSPs

Fixed-point DSP chip can generate real-time random noise. *An inexpensive, 16-bit, fixed-point DSP chip can generate real-time pseudorandom noise signals for testing the performance of telephony systems in the presence of noise.* Bill Salibrici, TeleSciences Co Systems; EDN, 4/29/93, pg 119, 4 pgs.

Graphics

Video decoder chip sports Windows scaling. *Integrated digital multistandard decoder and scaler simplifies desktop video designs.* Milt Leonard, Electronic Design, 5/3/93, pg 112, 2 pgs.

Image-processing chip set handles full-motion video. *Performing over 8 BOPS, a two-chip set can compress or expand video in real time.* Dave Bursky, Electronic Design, 5/3/93, pg 117, 4 pgs.

Memory

Novel IC merges SRAM and FIFO functions. *By combining the features of an SRAM and a FIFO buffer, a sequential-access RAM can match subsystem data rates.* Dave Bursky, Electronic Design, 4/15/93, pg 109, 2 pgs.

Flash-memory ICs redefine program and data storage for portable applications. *A single flash-memory chip can provide nonvolatile, updateable storage for execute-in-place program code. Multiple chips can create solid-state mass-storage systems.* Gary Legg, EDN, 4/15/93, pg 71, 4 pgs.

Touch-memory chips act as silicon labels that expand your LAN. JD Mosley, EDN, 4/15/93, pg 101, 1 pg.

Miscellaneous

Of workstations & supercomputers. *Figuring out which of the two types of machine best suits a problem requires constant attention as both classes continue to evolve.* Mark Furtney, Cray Research; George Taylor, Sun Microsystems; IEEE Spectrum, 5/93, pg 64, 5 pgs.

Goodbye Open Look, hello Motif. *Finally moved by a fear of NT, six of the largest Unix sellers settle on some standards. But much is left to be done.* Mark Cappel, Shalini Chatterjee, SunWorld, 5/93, pg 23, 5 pgs.

Processors

Sun unveils UltraSPARC as its next generation, V9-based SPARC chip. Shalini Chatterjee, SunWorld, 5/93, pg 30, 3 pgs.

Low-power µPs simplify design of portable computers. *Portable computer are changing the way people do business. At the heart of these compact mobile units are µPs with sophisticated power-management features that conserve battery life.* John Gallant, EDN, 4/29/93, pg 39, 6 pgs.

Motorola's 68360 communications controller moves to 32 bits. Ray Weiss, EDN, 4/29/93, pg 65, 2 pgs.

Communications controller handles nine protocols. *Full-featured protocol-processing engine and Ethernet transceiver implement WAN-to-LAN connectivity.* Milt Leonard, Electronic Design, 4/15/93, pg 53, 4 pgs.

Design low-cost, quick-and-dirty applications with 8-bit µCs. Ray Weiss, EDN, 4/15/93, pg 65, 4 pgs.

Transputer hits 50 MHz, goes superscalar. Ray Weiss, EDN, 4/15/93, pg 112, 2 pgs.

16-bit µC targets remote motor control. *The 8XC196MD, which integrates a 16-bit microcontroller with specialized motor-control peripherals, is capable of controlling both DC and 3-phase AC induction motors.* Ray Weiss, EDN, 4/15/93, pg 114, 2 pgs.

Programmable Logic

FPGA design services offer a helping hand. *Turning to an FPGA design expert can cut your development costs and speed your product to market.* JD Mosley, EDN, 4/15/93, pg 55, 3 pgs.

Dual-block PLD architecture offers speed and density. Doug Conner, EDN, 4/15/93, pg 102, 1 pg.

