AMD Upgrades Performance of 29200

Three New RISC Microcontrollers For Laser Printers, General Use

By Brian Case

AMD has upgraded its two-member 29200 RISC-based microcontroller family with three new devices. Announced at the recent Microprocessor Forum Europe in Munich, the new chips—the 29240, 29245, and 29243—combine the system integration of the 29200 with features of the higher-performance 29030, including on-chip cache. (For details on the 29200, see µPR 11/20/91, p. 1.) In addition, some peripheral functions have been slightly enhanced, and the ’240 and ’243 have a single-cycle 32×32 multiplier for DSP-like applications.

Figure 1 shows a block diagram of the new chips. All three are largely the same; the major differences are that the ’245—a low cost ’240 (AMD uses ’xx5 to indicate a low-cost version)—leaves off the data cache and fast multiplier, and that the ’243 eliminates the video interface and doubles the MMU size. The ’243 is intended to be a data-communications RISC microcontroller, while the other two are intended to be performance upgrades for the 29200 and the 29205 in laser printers. Table 1 summarizes the feature sets of the three new chips.

It is likely, at least at first, that all three chips will actually be identical silicon; this strategy has been used successfully with other 29000 processors, as well as by Intel and many other vendors. If the ’245 establishes a large enough market, AMD will build a unique, lower-cost die that leaves out the data cache and multiplier.

These new chips use a 196-pin PQFP package, compared to the 168-pin PQFP of the 29200 and the 100-pin PQFP of the 29205. Despite the significantly higher pin count, the new package pin-out is “foot-print compatible” with both the ’200 and ’205, which makes it possible to design a single board on which any of the three packages could be used.

The chips use a fully-static design and are specified with a 3.3V to 5V operating range. The low operating voltage coupled with external power-management circuitry are intended to make these chips appropriate for field-deployed telecommunications equipment, but these features could also help the ’240 find sockets in high-performance portable applications. AMD quotes a maximum current drain of 14 mA/MHz at 5.25V and 10 mA/MHz at 3.3V. Specifically for the communications market, all chips in the 29200 and 29400 family are available in industrial-grade temperature versions.

While the caches give the ’24x family a big performance advantage over the 29200, the higher clock rates can also boost performance. The 29200 is available in either a 16- or 20-MHz version, and the low-cost ’245 is offered only at 16 MHz. The ’240 and ’243, however, are available at 20, 25, and 33 MHz. AMD claims the instruction cache alone doubles performance compared to the 29200, and the 33-MHz clock rate makes another factor of two available to customers who need it.

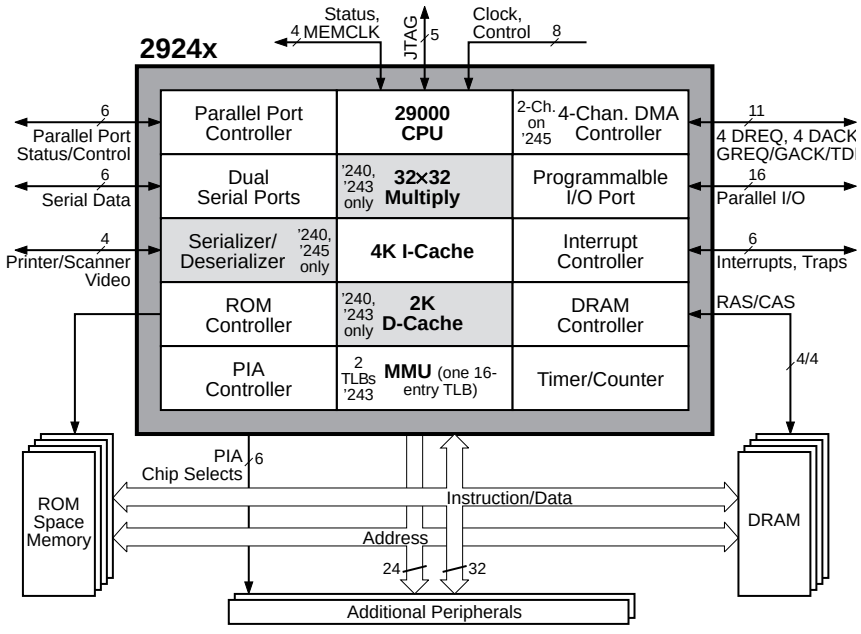

Figure 1. Block diagram of a 2924x system. The processor provides glueless interfaces to most memories and peripherals likely to be found in an embedded system.

On-Chip Caches

All three ’24x chips have a 4K, two-way set-associative instruction cache. This cache is based on the design of the instruction cache in the 29030. Reload is performed critical-word-first to allow the processor pipeline to restart as quickly as possible after a cache miss, and the cache has a valid bit for every word to minimize bus traffic due to reloads (only the instructions actually executed are fetched into the cache block and marked valid). As with the cache in the 29030, half the cache can be locked and preloaded to guarantee rapid access to important code.

The ’240 and ’243 have a second on-chip cache: a 2K, two-way set-associative

data cache. As with the instruction cache, reloads are performed critical-word-first, and the critical data is forwarded directly to the pipeline without first being stored in the cache ("load-through" in AMD lingo). Refills use burst mode with a wrap-around address sequence. The data cache uses a write-through policy, and a two-entry write buffer is implemented to let the processor continue executing after the stores are posted.

As on the 29030, all cache tags, valid bits, and data storage for both caches are visible to software for testing.

System Integration Features

The '245 implements the same set of system peripheral functions as the 29200: glueless DRAM and ROM control, two-channel DMA engine, 16-line programmable I/O port, peripheral-interface adapter, parallel port, serial port, video serial interface, and interrupt controller. The '240 and '243, however, go a little further by including four DMA channels and two serial ports.

As on the 29200, the DRAM controller can handle four banks of memory, and each bank can be a different size and width, either 16 or 32 bits wide. New on the '243 is support for DRAM parity. The DRAM interface is designed to exploit a two-cycle-first/single-cycle-burst access pattern. This allows the 2-1 pattern using 80 ns DRAMs at 16 MHz, 70 ns at 20 MHz, and 60 ns at 25 MHz. The ROM controller maintains its ability to handle four banks, where each may be of a different size, have different timing, and be either 8, 16, or 32 bits wide.

The DMA channels have been enhanced. They are now capable of queued reload, and the fly-by mode of operation can deliver up to 100 Mbytes/s throughput.

Another feature, borrowed from the 29030 and offered only on the high-end '240 and '243 chips, is the ability to run the bus at half the processor speed. As in the PC world, this has the benefit of combining a cheaper system design with a fast processor, or allowing an existing slow system to be upgraded to a faster processor without system redesign.

All three chips have an MMU with a full-blown TLB instead of the simple address-offsetting capability of the 29200 MMU. The page size of the TLB can be set to any value from 1K to 16M in powers of four (1K, 4K, 16K, etc.). The '240 and '245 each have a single 16-entry TLB, while the '243 has two 16-entry TLBs.

AMD says its customers in the communications industry requested the extra TLB and the on-chip parity of the '243. The fact that each TLB can be set for a different page size allows a more efficient memory organization to be designed.

The TLBs translate both memory addresses and on-chip-peripheral addresses. Thus, when using a protected operating system, on-chip peripherals can be protected just like memory regions.

The on-chip, single-cycle multiplier of the '240 and '243 make them usable in some applications that would have required a DSP chip. The multiplier can perform a 32×32 multiply and deliver a 32-bit result in one cycle. A 64-bit result takes two cycles. Consequently, a 32-bit multiply-accumulate can be performed on the '240 or '243 in two cycles with two instructions.

Price & Availability

The 29240 is available now at clock speeds of 20, 25, and 33 MHz. The 20 MHz part costs $88 in quantities of 1000. The 29245 is available now at a clock speed of 16 MHz for $69 in quantities of 1000. The 29243 is also available now in clock speeds of 20, 25, and 33 MHz; the 20-MHz part costs $97 in quantities of 1000.

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Conclusions

In terms of providing an evolutionary upgrade path for existing 29200-based systems, the 2924x family clearly succeeds. The '245 provides a simple way to double processor performance for not much more cost—the 29200 costs less than $50 compared to $69 for the '245. The high-end members, the '240 and '243, should finally provide some strong competition for the the MIPS-based 3051/3052 processors. Compared to the large caches (16K instruction, 4K data) of the 3081, however, the caches on the '240 family are still rather small.

AMD also seems to be taking small steps to test new markets with the 2924x family. The low-voltage operation, static implementation, and on-chip parallel multiplier may allow AMD to successfully pitch its RISC microcontrollers in portable applications that require significant processor performance. Though it may be too late to capture many of the general-purpose pen-based system sockets, the future may provide opportunities to win business in dedicated, special-purpose hand-held applications. ♦

Feature	29200	29205	29240	29245	29243
Instruction Cache	none	none	4K	4K	4K
Data Cache	none	none	2K	none	2K
MMU	Some addr. remapping	Some addr. remapping	16-entry TLB	16-entry TLB	Two 16-entry TLBs
DRAM Parity	No	No	No	No	Yes
Video Interface	Yes	Yes	Yes	Yes	No
Serial Ports	One	One	Two	One	Two
DMA Channels	Two	Two	Four	Two	Four
Bus Speeds	1× only	1× only	1×, 2×	1× only	1×, 2×
Hardware Multiply	No	No	Yes	No	Yes
Max. Frequency	25 MHz	16 MHz	33 MHz	16 MHz	33 MHz

Table 1. Feature comparison of the 2924x family and the original 29200 and 29205.

