T9000 Transputer Begins Sampling

Complexity Causes Schedule Delays, Increased Transistor Count

By Linley Gwennap

Like others before, Inmos has discovered that designing a superscalar microprocessor is inevitably more difficult than it first seems. Its newest Transputer, the T9000, was originally expected to ship in 1Q92 at 50 MHz. Inmos now plans to make initial shipments at 40 MHz in 4Q93, with 50-MHz parts expected sometime next year.

The T9000 (see µPR 5/15/91, p. 9) extends the capabilities of its predecessor, the T805, in several ways. The new chip can execute up to eight instructions per cycle; the T805 is a scalar processor. Other important improvements include faster links and virtual channels.

Design Problems Added Complexity

Inmos initially expected the T9000 to use 2.2 million transistors, but as the design progressed, the engineers needed to add additional circuitry to detect and handle dependencies among the eight instructions that potentially could be issued on each cycle. Because the Transputer architecture uses variable-length instructions, decoding and grouping these instructions is more complex than in a standard RISC design.

To simplify the design and improve the architecture, the team decided to break binary compatibility with the T805. The Transputer architecture (see µPR 4/17/91, p. 10) includes a process scheduler, which is implemented in hardware on the T805. The T9000 changes this process model, forcing old applications to be recompiled for the new chip. Since Transputers have been used primarily in embedded applications and a few parallel systems, this change will mainly impact developers and not end users.

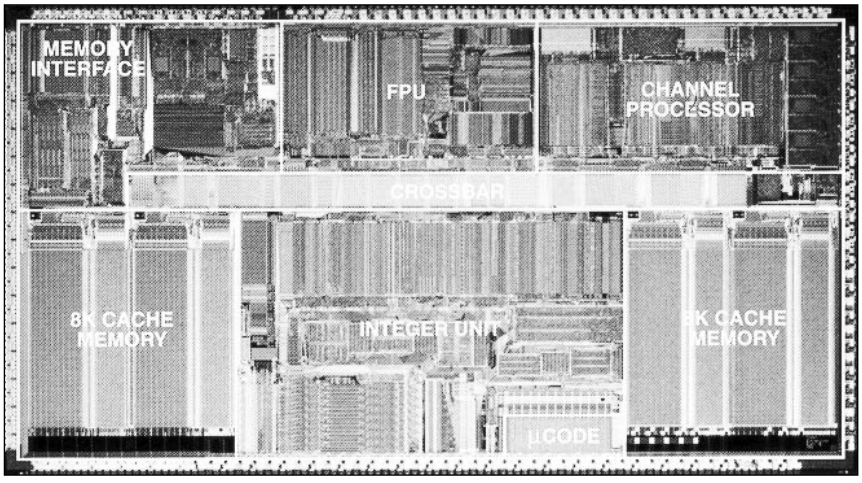

Figure 1. The T9000 uses 3.3 million transistors on a 10 × 18 mm (400 × 700 mils) die.

The first complete silicon was received in September, 1992. It uses 3.3 million transistors, 50% more than originally planned, on a 180-mm^2 die (see Figure 1). The first parts (A-step) had several problems. The B-step parts have a much smaller bug list but are limited to 20 MHz; these parts are currently being sampled. The C-stepping is expected to fix functional problems except for some floating-point bugs, and increase the clock speed to 40 MHz; this version will be used for initial shipments. Inmos expects to produce fully-functional 50-MHz T9000s in 1994.

Production parts initially will cost about $500 and use under 8 watts at 50 MHz. In 1995, the company plans to move the design to a 3.3V, half-micron process, providing a significant reduction in both power and price. By that time, Inmos hopes to sell the chip for about $100.

T9000 Instruction Dispatch

The capabilities of the T9000 design have changed little since the original technology disclosure nearly two years ago. The most striking feature is the eight-instruction dispatch, which at first glance appears more capable than any current microprocessor. Because of its unusual instruction set, however, the T9000 was forced to a very wide instruction dispatch simply to keep pace with other architectures. The Transputer architecture is stack-based, making a group of its instructions equivalent to a single RISC (or CISC) instruction.

To achieve its maximum issue rate, the chip must make full use of its two load pipes and two ports into the workspace stack. It can also perform one ALU operation (integer or floating-point), one jump, and one store. The eighth instruction is a special case; the sequence "eqc 0; cj" (check if zero, jump if false) is implemented in hardware as if it were a jump-if-not-zero instruction. This special case is useful because the Transputer architecture does not have a jump-if-not-zero instruction. All of the eight instructions must also use the single-byte encoding.

Figure 2 shows an actual code sequence for which the T9000 would issue eight instructions in a single cycle. Both the T9000 instructions and typical RISC instructions are given. From this comparison, one might conclude that the T9000 is equivalent to a three-way superscalar RISC processor, but no current RISC chip could issue two load instructions simultaneously. (Intel's Pentium chip has this capability.) Furthermore, the

Price and Availability

The T9000 is currently sampling at $695. It will begin shipping in 4Q93 at a price of $495 in 1000s. The chip uses a 208-pin PQFP. Contact Peter Uehlecke at SGS-Thomson Microelectronics, 617/259-0300.

data dependencies between the loads and the branch would prevent those instructions from being grouped in processors with a typical RISC pipeline, although they could execute in parallel with other non-dependent instructions.

Of course, this example is optimized for the T9000. In most cases, the Inmos chip will not come close to its maximum issue rate. Realizing this, the designers provided a fetch rate of four bytes per cycle, half of the peak issue rate, into the instruction prefetch buffer. The maximum sustained rate is therefore four instructions per clock cycle, assuming no multibyte instructions.

Crossbar Connects Key Features

The T9000 uses a crossbar of four 32-bit buses providing for instruction fetch, two loads, and one store per cycle. It connects the CPU to the 16K on-chip cache, the virtual channel processor (VCP), and the programmable memory interface (see Figure 1). The cache is organized in four banks and can service four accesses per cycle as long as each is to a different bank. For real-time applications, the cache can also be configured as on-chip RAM. The chip does not directly support a second-level cache.

The memory interface directly controls up to 32M of DRAM with a variety of configurations and timing parameters. The interface can transfer 64 bits per cycle at one-half of the CPU clock rate.

The channel processor includes four serial "links" to connect to other T9000s. The data rate is 100 Mbps, a five-fold improvement over the T805. The VCP also provides "virtual channels" that allow different software processes to easily share the same physical link.

Conclusions

The T9000 is an impressive technological feat. It has the highest transistor count of any microprocessor yet announced, and its die size is modest for such a complex chip. Its power consumption is also lower than other devices of comparable complexity and clock speed. Its market penetration, however, will be hampered by several factors.

Despite parent company SGS-Thomson's claims, the T9000 is not the world's fastest single-chip processor, even when its 200 peak native MIPS rate is considered. On Dhrystone 2.1, the as-yet-unseen 50-MHz T9000 has been simulated at 36 VAX MIPS, higher than a 33-MHz 486 but much lower than the 100-MIPS Pentium, a chip of comparable complexity. On larger programs, the T9000's performance will suffer without an external cache.

```
C CODE:
    if (text[i] \= target[6])
        something ;

TRANSPUTER CODE (8 bytes):
(the following instructions will issue in one cycle on the T9000
assuming that "i" is already loaded on the evaluation stack.)
    ldl text            ; load base address "text"
    wsub                ; calculate address of text[i]
    ldnl 0              ; load text[i] from non-local memory
    ldl target          ; load base address "target"
    ldnl 6              ; load target[6] from non-local memory
    diff                ; subtract (gives 0 if equal)
    eqc 0               ; check result (gives 0 if not equal)
    cj else_clause      ; conditional jump if zero (not equal)

PA-RISC CODE (12 bytes):
    ldwx r1(r2,0),r3    ; load text[i]
    ldw 6(r4,0),r5      ; load target[6]
    comb,<> r3,r5       ; compare and branch if not equal
```

Figure 2. For this code fragment, the T9000 requires eight instructions but can issue them all in a single cycle; a typical RISC would use three instructions but could not group them.

The Transputer continues to suffer from its reputation as a off-beat approach that is more popular with researchers than commercial users, but its design wins show that this may be changing. It also suffers from the lack of a marketing campaign and applications support infrastructure, especially in the US, comparable to that fielded by AMD, Intel, and Motorola.

According to Inmos, about one million Transputers are in use, with about one-fourth of them shipped in 1992. The company expects to ship about 500,000 units in 1993. While this trails the top embedded RISCs (the i960 and AMD's 29000) and is far less than Motorola's 68000 shipments, Transputers have been more successful than their low profile (at least in the US) indicates.

The Transputer is most compelling in multiprocessor applications that can use its unique links and distributed task model. For example, massively parallel systems are used for applications such image processing. Other parallel applications include database servers, ATM servers, video-compression systems, and compute servers. These types of applications always need more performance, and the T9000 is a welcome upgrade. At the other extreme, the chip has found some uniprocessor applications, such as GPS receivers and disk drive controllers. These designs often use the serial links for application-specific I/O.

The Transputer is now facing stiff competition in uniprocessor applications from embedded RISCs at the high end, and from integrated 68300-family chips at the low end. The T9000 helps this competition by extending the performance range, but at the introductory price, the chip's price/performance does not seem to compare favorably to other embedded processors. Inmos must rapidly drop the price to make the T9000 more attractive.♦

