Most Significant Bits

Mitsubishi to Manufacture, Sell Alpha Chips
DEC has licensed its Alpha architecture to Mitsubishi Electric (Melco), allowing the Japanese firm to second-source Digital CPU designs and to design its own microprocessors. Mitsubishi does not expect to market Alpha chips until the end of 1994 and will probably start with the 0.5-micron version of DEC's forthcoming "Low-Cost Alpha" (LCA) chip *(see **061506.PDF**)*.

It isn't clear who will buy these chips, although Digital indicated it will meet some of its internal demand with Mitsubishi parts. DEC is "working on" several customers for LCA, but as yet has no firm deals. Both companies are presumably counting on Alpha's success as a Windows NT platform.

Mitsubishi also expects to design its own Alpha processors, probably focusing on the embedded market. Melco is a leading supplier of microcontrollers but ships mainly 8-bit and 16-bit parts. The company's only experience with 32-bit CPU design has been its participation in the ill-fated Tron project.

Mitsubishi is also a member of the Precision RISC Organization (PRO) and buys PA-RISC boards and systems from Hewlett-Packard. HP believes that this relationship will not change in the near future. Toshiba is similarly schizophrenic; its systems group uses SPARC while its semiconductor group sells MIPS processors.

DEC Announces 200-MHz Chip Availability
Digital also confirmed that it will begin volume shipments of 200-MHz Alpha processor chips in July, meeting a commitment made last fall. To reach this milestone, the company has fine-tuned its CMOS-4 process to produce 0.68-micron devices, a 10% shrink from the original specification. With the new process, DEC believes it will have good yield on Alpha chips at up to 200 MHz.

The company is currently shipping small volumes of 200-MHz DEC 10000 systems using chips from the old process. The new chips are available now in sample quantities at a steep $3495 each. In July, volume pricing drops to $1231 in quantities of 10,000.

The company rates the 200-MHz Alpha chip at 106 SPECint92 and 200 SPECfp92, based on its performance in the DEC 10000 *(see **070401.PDF**)*. That system is a very high-end implementation, however, with 4M of external cache; a volume workstation design would have about 5%–10% lower performance.

Sharp to Sell ARM Processors
Sharp Electronics has been licensed to manufacture and market ARM processors by Advanced RISC Machines. The Japanese company gives ARM a truly global presence by joining with the other two ARM vendors, US-based VLSI Technology and GEC Plessey in Europe.

The addition of Sharp increases the worldwide manufacturing capacity for ARM chips in time to meet the expected high volume of products such as Apple's Newton and 3DO's interactive video system *(see **0701MSB.PDF**)*. Sharp will be building the Newton, so it can supply itself with chips. Sharp can also help attract other Asian consumer-electronics companies to the 3DO platform or other ARM-based applications. ARM recently gained another ally in Japan, when Nippon Investment and Finance made a $900,000 equity investment.

TI Announces 3.3V, 33-MHz 486DLC
Texas Instruments is now sampling the TI486DLC-V33, a 33-MHz, 3.3V version of the 486DLC microprocessor that it builds under license from Cyrix. Cyrix itself has offered 3.3V versions of its processors only up to 25 MHz so far; TI says that its enhanced process enables its chips to run at 33 MHz at the lower voltage. The new TI chip will enable vendors of notebook systems to build higher-performance products while maintaining low power consumption, provided they can get the 3.3V DRAMs and other components needed to complete a low-voltage design. Pricing has not been released, but TI expects the 3.3V chip to sell for a small premium over the $99 price of the 33-MHz, 5V version (in 1000s). Volume production is planned for the third quarter.

MicroUnity Building High-Speed Fab
Ever since MIPS cofounder John Moussouris started MicroUnity Systems Engineering in 1989, the industry grapevine has been rife with speculation on what the company is up to. Four years later, the company has grown to 60 employees and remains as secretive as ever, but word has leaked out that the company is building its own semiconductor fab facility in Sunnyvale, California. Sources indicate that the fab is not yet complete, and that the company will also use outside foundries.

Several patents issued to the company last year provide a glimpse into the technology it is developing. The patents describe a very-high-speed BiCMOS process and related technologies. A novel planarization process enables high density, and special efforts have been made to allow dense wires as well as transistors. One particularly exotic technique is to selectively "air bridge" connecting traces by etching out the material below the metallization, reducing the capacitance of the wire and allowing higher switching speeds. Clock rates well above 1 GHz are rumored to be possible with this technology.

Of course, a high-density, high-speed process is like-

ly to generate plenty of heat, and the company has also patented a heat-exchanger design that uses a stack of laminated, thin copper plates etched to provide channels for a cooling liquid.

Just what the company is building with all this technology remains shrouded in mystery. Officially, the company will say only that it is developing "ultra-high-bandwidth digital systems." The company is funded by several corporate partners, none of which it will name; rumors have included Hewlett-Packard, DEC, and Cray. One rumor is that the products are related to video signal processing, and that a cable TV company is a major investor. Product shipments are not expected until 1995.

MIPS Pumps Up R4400 Performance Numbers

Although we recently expressed some disappointment that MIPS' R4400 didn't meet its initial performance goals *(see **0702MSB.PDF**)*, apparently the company wasn't done yet. The 150-MHz Indigo^2 was originally rated at 82 SPECint92, but measurements on a new 150-MHz prototype system with 4M of 10-ns cache show the chip reaching 94.2 SPECint92 *(see **070401.PDF**)*. Similarly, SPECfp92 performance is up from 86 to 105.2. MIPS attributes part of the increase to the larger cache and part to compiler tuning. The chip itself is now available in volume at 100 MHz, with 150 MHz parts due to sample soon and ship in volume by 3Q93.

Bob Miller Heading New Workstation Venture

Robert Miller led MIPS in its heyday and is currently CEO of the MIPS Technologies division of Silicon Graphics. Now, he has founded a new venture-backed workstation company called NetPower Systems. Miller declined to discuss the company's product plans, but sources indicate that NetPower will market low-cost MIPS workstations made by OEM suppliers. For the moment, at least, Miller retains his seat on SGI's board and his position as head of the MIPS architecture committee, but is expected to be replaced at MIPS Technologies.

OPTi Introduces Chip Set for 486 S-Series

OPTi has introduced a single-chip system-logic device for Intel's unannounced "S-Series" processors. Curiously, the chip set is ahead of the processor family itself, a line of 486 microprocessors that will provide static operation, system management mode, and low-voltage operation. These chips are expected to replace the SL line with a less-integrated approach that gives chip-set makers such as OPTi a bigger role in the portable system market.

The 82C463 single-chip notebook (SCNB) controller provides all the usual PC system logic and a variety of power-management functions in a single 208-pin chip. According to OPTi, the only other devices required (in addition to the processor and memory) are 6 glue chips, a real-time clock/calendar chip, and a keyboard controller. The SCNB also supports VL-Bus slave devices.

To support the S-Series, the OPTi chip provides an assortment of idle timers and an SMI (system management interrupt) output to trigger the processor's power-management software. For processors that do not support SMI, the chip also includes a simple microcontroller that can execute power-management software without interrupting the main processor.

The SCNB also controls the processor's clock; according to OPTi's documentation, the new Intel CPUs will consume only 50 µA when the clock is stopped. The OPTi chip also implements clock-stretching to reduce power consumption; when the processor is waiting for an external access to complete, the clock is stopped until "ready" is asserted. This reduces processor power consumption by 20 to 40 mA, according to OPTi, but does not affect performance, since program execution does not continue in any case until ready is asserted.

The SCNB 82C463 can operate at either 3 or 5 volts. It is in production now and is priced at $25 (10K).

Microsoft Launches Plug and Play Initiative

Spurred on by Apple's advertising attack on the difficulty of adding hardware to PCs, Microsoft has been working with Intel, computer makers, and add-in board vendors to eliminate the board configuration nightmare. The problem is familiar to anyone who has ever added a board to a PC: you often have to find unused IRQ and DMA levels, set jumpers, select addressing ranges—and then pray that your system will still boot. Apple solved this problem very nicely in the Macintosh, and some newer PC buses, such as Micro Channel and PCI, have also tackled it. The original PC did nothing about automatic configuration, however, and the lack of any PC vendor with enough clout to lead changes in the architecture has hampered advances.

Microsoft, which has the most clout in the PC industry, has therefore taken it upon itself to tackle some of these problems, and Plug and Play is one example. (Another is the Extended Capabilities Port, an enhanced parallel printer port, which Microsoft developed in collaboration with Hewlett-Packard.) Microsoft intends to apply the Plug and Play concept to all PC buses, but it is starting with ISA because of its pervasiveness.

The Plug and Play protocol requires that all add-in boards power-up in a mode in which they do not respond to normal bus activity, so there can be no boot-up conflicts. The auto-configuration process, which can be managed by the card's driver software or by system software that Microsoft will supply, consists of isolating each card, reading its resource requirements, and then assigning resources to all cards. The Plug and Play specification includes a clever technique (too complex for us to describe here) for isolating each card and creating a pseudo-geographic addressing mechanism, which is non-trivial

since there is no support for this in the ISA bus.

Microsoft is soliciting comments on the specification and hopes to develop a final version later this spring. If all board vendors support this, it would be a big step forward for PC users. To request a copy, call Mike Flora at 206/882-8080 or send e-mail to *plugplay@microsoft.com*.

Intel Releases PCI License, but is it Enough?

In an effort to ensure that PCI remains an open standard, the PCI SIG steering committee is working to alter the wording of Intel's patent license, committee member AMD has told *Microprocessor Report*. Intel's recently-issued licensing agreement, intended to convince the industry that it intends to make PCI open, has instead fueled suspicions that Intel isn't showing all its cards. The agreement reads as follows:

> "Intel Corporation hereby grants to Registered User (any entity who at any time has requested the PCI Specification and paid the order fee required by the PCI Special Interest Group) a paid-up, royalty-free, non-exclusive, irrevocable, worldwide license under all Intel patents issuing from the following three pending Intel patent applications titled:
> 1) 'A Signaling Protocol for a Peripheral Component Interconnect,'
> 2) 'Improved Bus with Commands for Optimizing Bridge Buffer Management,' and
> 3) 'Configuration Space Enable/Disable Mechanics,'
> to design, develop, manufacture, use and sell systems and components compliant with the PCI Specification (Rev. 1.0 and prior revisions).
> "No other license, express or implied, to any other Intel patent or patent application or other intellectual property is granted or intended hereby."

In particular, other steering committee members would like to broaden the license to cover any existing, pending, or future Intel patent needed for PCI systems and components. Intel specifically avoided granting such a broad license, blaming its lawyers, who insisted on avoiding any ambiguity in the terms. The company has consistently stated its intent that PCI be open.

The current license does not include patents that Intel has pending on its PCI chip set; while these patents are not essential to PCI, they could prove troublesome to other chip-set makers, who may have to design their chip sets before the content of the patents becomes known. AMD would also like to extend the patent license to all future revisions of PCI; Intel has agreed to make this modification in Revision 2.0 this summer.

Dell Using Patent to Slow VL-Bus

In what appears to be a blatant attempt to slow the VL-Bus momentum while it readies PCI systems, Dell Computer has sent notices to numerous companies building VL-Bus systems alleging that these systems violate a Dell patent. The patent in question, No. 5,036,481, was granted on July 30, 1991 and appears to cover the concept of putting a second connector in-line with the standard bus connector to provide access to a separate, high-speed expansion bus.

Dell is a VESA member and is one of the companies that voted to ratify the VL-Bus standard. As part of the ratification process, all members were required to identify any intellectual property that might affect use of the proposed standard, and Dell's representative to VESA signed a statement indicating no knowledge of such conflicts.

Dell can expect a vigorous effort to overturn the patent, as well as challenges based on its failure to identify the patent conflict during the standardization process. Several observers believe that prior art exists on this idea. More fundamentally, this patent should surely fail the test of non-obviousness. For the patent system to protect obvious, straightforward ideas such as putting two connectors in line for access to two buses is clearly counterproductive. Nevertheless, Dell may well succeed in slowing down the adoption of the VL-Bus, causing significant harm to competitive PC vendors.

PowerOpen Formally Announced

Following in the footsteps of other RISC architectures, PowerPC now has its own vendor coalition. IBM, Apple, and Motorola have formed PowerOpen, an independent company chartered to coordinate architectural development and attract software vendors. The group—which also includes Groupe Bull, Thomson-CSF, Harris, and Tadpole—plans to develop ABI and API specifications for PowerPC and to develop validation suites.

The PowerOpen ABI/API will be based on IBM's flavor of UNIX (called AIX/6000) running on PowerPC. It will support Motif as well as the new Macintosh Applications Services (MAS), which turns any window into a Mac-like desktop. MAS provides standard System 7 features such as cut-and-paste, folders, and the Finder. It also executes any Mac application using a combination of 68040 emulation and native Toolbox code.

Sources indicate that, in pure emulation mode, the first PowerPC 601 systems will run Mac programs at about the speed of a 25-MHz 68030. Since these applications often spend 70% or more of their time in the toolbox, which will run natively, overall performance should be about the same as a 25-MHz 68040. Fully-native applications could see a more than 2× improvement over the fastest 68040. The first systems supporting the full PowerOpen environment with MAS are not expected until 1Q94. ♦

