Sun Details Extensive Plan for SPARC CPUs

V9-Compatible "UltraSPARC" Due in 1995 at 140 MHz

By Linley Gwennap

Responding to criticisms of SPARC performance, Sun has unveiled a massive effort to improve its processors over the next few years. The company claims to be working on no fewer than nine CPU projects currently and to be spending $500 million per year, in conjunction with its SPARC partners, on new processor and IC process development.

Although Sun had previously shared credit with its partners on various SPARC designs, Sun is now taking full responsibility for all of the previous CPU designs used in its SPARC systems. (HyperSPARC is the only major design not done by Sun, and Sun has not yet announced plans to use it.) The company plans to continue to be the driving force behind new SPARC processors. Sun also emphasized the openness of the architecture, with $99 licensing and multiple sources of processor chips, and encourages other chip vendors to develop SPARC chips for market niches that are not addressed by Sun's master plan.

The expected product rollout, shown in Figure 1, includes three families. The first two, microSPARC *(see **061402.PDF**)* and SuperSPARC *(see **060701.PDF**)*, were introduced in 1992 for the low end and mid-range, respectively. Sun will continue to improve and enhance these designs over time. The new family, called UltraSPARC, will debut in early 1995 as a high-performance successor to SuperSPARC and will implement the SPARC-V9 architecture *(see **070201.PDF**)*.

MicroSPARC Anchors the Low End

Sun expects to rely on microSPARC at the low end for years to come. The current version is manufactured by Texas Instruments (TI) in a low-cost 0.8-micron CMOS process. It is shipping in the $4295 SPARC Classic at 50 MHz. The frequency is not limited by the core CPU but by the SBus interface, which is constrained to run at half of the CPU clock rate. SBus itself is limited to 25 MHz. By simply modifying the chip to clock the SBus at 1/3 of the CPU frequency, Sun expects microSPARC to run at 60 or even 75 MHz in systems that ship later this year, boosting performance to about 40 SPECint92. Floating-point performance for the microSPARC chips is about the same as integer on the SPEC ratings *(see **070401.PDF**)*.

The next generation, microSPARC-2, will use a similar scalar processor core implemented in a half-micron, three-layer-metal process. The integer unit will be enhanced to handle branches better, possibly through branch folding, and the floating-point timings will be improved somewhat. The new process will allow the caches to be quadrupled to 16K of instruction and 8K of data cache. Power management features and 3.3V operation will make the new chip more attractive in portable applications. Sun has not yet identified the manufacturer; Fujitsu and TI are rumored to be in the running.

MicroSPARC-2 is slated to debut at 70 MHz initially, with first system shipments in 2Q94. Although that clock frequency is slightly lower than that of its immediate predecessor (see Figure 1), the larger caches and functional enhancements should provide slightly better performance. By early 1995, the chip is expected to hit 100 MHz and over 60 SPECint92.

A third-generation microSPARC will include external cache support. In addition, process enhancements may push the frequency as high as 125 MHz by 1996. Sun expects the microSPARC family to eventually top out at nearly 100 SPECint92.

Faster SuperSPARC Coming Soon

TI is currently shipping 40-MHz SuperSPARCs in volume based on the second complete mask set of the part. (Several intermediate versions changed only the metal layers.) Sun is testing samples built using a third mask set, which TI has manufactured using a tweaked version of the original process. The new 0.7-micron BiCMOS process is expected to produce parts in the

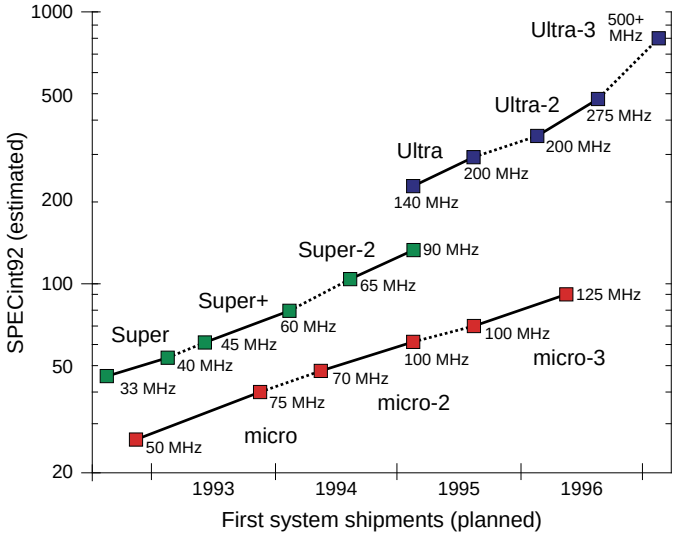

Figure 1. Sun's plan for future SPARC processors includes the microSPARC, SuperSPARC, and UltraSPARC families. (Source: data from Sun with adjustments by µPR)

45–50 MHz range later this year and hit 60 MHz in 2Q94, topping out around 85 SPECint92 and 115 SPECfp92. The 0.7-micron parts, called SuperSPARC+, are functionally identical to the original design and will continue to be manufactured by TI.

Sun is also working on an enhanced version of the chip called SuperSPARC-2. This design is targeted for a 0.6-micron BiCMOS process but will remain at 5V. Sun will make some improvements to the integer and floating-point units but will retain the basic three-issue design. One specific improvement will be the ability to launch two FP instructions per cycle, similar to current POWER and PA-RISC processors. The design will not incorporate the new SPARC-V9 instructions.

SuperSPARC-2 is expected to debut in 3Q94 at 65 MHz. Sun hopes the part will achieve about 120 SPECint92 and 160 SPECfp92. By 1995, the chip is projected to reach 90 MHz, or about 150 integer SPECmarks.

UltraSPARC Goes to 64 Bits

The new UltraSPARC design is intended to provide the ultimate in SPARC performance. It will be the first Sun design to implement the 64-bit SPARC-V9 architecture, although HaL is widely expected to ship V9-based products this year. The new design will be able to launch up to four instructions per cycle, one more than SuperSPARC, including up to two floating-point instructions. It will probably implement dynamic branch prediction as well as V9's static branch prediction.

A major change from the current design is that Sun plans to aggressively push the clock frequency. Initial versions of the chip, due in early 1995, are slated to run at 140 MHz using a 0.5-micron, four-layer-metal CMOS process. Later versions are planned at 200 to 275 MHz, with UltraSPARC-3 tipping the scales at over 500 MHz. Sun has not yet announced its foundry for this design.

The 140-MHz UltraSPARC is projected to perform at about 230 SPECint92. Sun foresees more emphasis on floating-point performance in future applications, so it is designing the UltraSPARC chips such that their SPECfp92 rating will be about 50% higher than the integer rating. Sun hopes that UltraSPARC-2 will reach over 400 SPECint92 by the end of 1996.

The UltraSPARC project has been underway for over a year, and the basic design parameters are now solid. Tape release is not planned until 1994. Sun has not released information about target die size, but expects that the processor will be more expensive than SuperSPARC, indicating an even larger die.

Sun Vows to Solve Credibility Problems

Sun has outlined an ambitious plan to extend the SPARC processor family. While the company swears that all of these programs will meet or exceed the expectations outlined here, it has had problems meeting its forecasts in the past. The original SuperSPARC program was 12 to 18 months late by some estimates. Worse yet, the frequency declined over time from as high as 80 MHz in initial projections to 36 MHz in first shipments. To be fair, other companies have also failed to meet projections made two or more years in advance, as such estimates are inherently optimistic.

That being said, the SPARC roadmap as a whole appears reasonable, particularly the microSPARC and SuperSPARC follow-ons. These two families are extensions of known designs into future manufacturing technologies. The UltraSPARC goals seem aggressive, as they indicate a 50% increase in clock frequency over SuperSPARC-2 in the same timeframe, plus a 25% boost in instructions per cycle. Sun argues that its experience with the highly-superscalar SuperSPARC design will allow it to more easily push the clock rate of UltraSPARC. At least it knows what not to do.

Can SPARC Become Competitive?

The roadmap shows little hope for Sun regaining a performance edge any time soon. If it can push a 50-MHz SuperSPARC+ out the door by this summer, it could avoid the embarrassment of seeing Pentium systems outperform its fastest workstations on integer benchmarks, but other RISC vendors will still hold a significant lead in both integer and floating point. Sun's plan shows SuperSPARC improving at about 60% per year, which is the same curve that other major architectures are riding. Thus, even as SuperSPARC continues to improve, new chips from DEC, HP, MIPS, and IBM will probably surpass it.

UltraSPARC is Sun's next opportunity to make a major gain against its competitors. Its target of 230 SPECint92 is a formidable goal and lies at the high end of projections for DEC's EV-5 and the MIPS T5 project, also due around early 1995. If Sun can deliver (and who knows if the other vendors will meet their goals?), it could return SPARC to the forefront in performance.

Even if UltraSPARC doesn't vault past the competition, Sun's market share may not significantly shrink; for over two years, the company has managed to retain its leading workstation status without having leadership performance. In the high-volume markets, price and price/performance are more important; the microSPARC family will carry the load in this area. At the high end, Sun may be able to use multiprocessing.

Another critical factor is software availability. Sun has more applications than any other RISC platform, fueling its success. This advantage may not hold, however, after the arrival of Windows NT, which will allow thousands of Windows programs to run quickly and easily on MIPS and Alpha systems. At some point, Sun may need to re-examine its software strategy; its new roadmap does not indicate any little-endian processors. ♦

