PCMCIA Interface Chips Follow Intel's Lead

Vendors Hoping ExCA Standardization Helps Market Explode

By Brian Case

The current standard for credit-card-sized computer peripherals—PCMCIA 2.0—evolved from an early design for memory cards. These small cards were intended to provide memory expansion and to connect more or less directly to an internal processor bus. Over time, it became clear that the small form factor could accommodate many important peripheral functions as well, and a group—the PCMCIA (Personal Computer Memory Card International Association)—formed to set standards for the emerging PC Card technology.

Though its roots as a memory connection are still evident *(see **061604.PDF**)*, the PCMCIA electrical interface is a capable expansion bus with the ability to accommodate multiple memory and peripheral cards in a single system. Because the interface is appropriate for many popular peripherals and the small PCMCIA form factor is so attractive, four semiconductor vendors—Cirrus Logic, Databook, Intel, and Vadem—are offering interface chips to tap the huge market potential. These chips can ease the integration of PCMCIA interfaces into a variety of computers, from palmtop to desktop machines.

As a further catalyst to market development, Intel is promoting its ExCA (Exchangeable Card Architecture) definition for x86-based PCMCIA hardware and software. As a specific implementation of some of the

Overview of Interface Chip Functions

The purpose of PCMCIA interface chips is to control one or more PCMCIA sockets by translating a system bus protocol to the PCMCIA bus protocol. Since this is a PC-clone-centric world, the designers of these chips have chosen ISA as the system bus.

Architecturally, the chips are fairly simple. They contain a multitude of registers for storing configuration information and status bits and internal buses for routing control and data. As with PC chip sets, the biggest headache for chip designers is package pin-count limitations.

The major differences among these interface chips fall into three categories: the number of socket interfaces (one or two), the presence or absence of full address and data buffering (for hot insertion/removal), and register-level compatibility with the Intel 82365SL. The PCMCIA definition of hot insertion/removal is "without removing card power," but many in the industry are using the definition "without rebooting the machine," i.e., "without removing power to the machine." This is an issue since some chips support hot insertion/removal as long as there is no card activity while others have full signal buffering and power sequencing.

One function of these chips is dictated by the addressing-range incompatibility between the ISA bus and the PCMCIA bus: PCMCIA specifies a 64M address space while ISA has only 16M. To allow access to the full 64M space, all these chips implement base/offset memory and I/O address-mapping windows similar to those available with LIM/EMS hardware.

Another important function of these interface chips is interrupt steering for PC Cards with I/O devices. The interrupt signal from a card can be directed to any of the ten ISA interrupt lines under program control. I/O address windowing, together with interrupt steering, lets these chips make PC Card I/O hardware look as if it used standard motherboard ports—such as COM1 in the case of a modem.

One of the chief applications for PCMCIA technology is in low-power, portable equipment. Accordingly, PCMCIA interface chips have features, such as stopping internal clocks, to reduce power consumption when sockets are empty or cards are installed but idle.

Operational Overview

In a system with a PCMCIA chip, operation begins at boot time with a system software module that initializes the interface chip(s). Socket services software drivers isolate particular register organizations from higher-level software.

The chips can be configured to apply power to a card as soon as it is installed, or to cause an interrupt and let software turn on card power. Typically, a card-insertion interrupt would be enabled to let the system know that a card has been installed or removed regardless of automatic power-on.

Once a card has been installed and system software is alerted to its presence, the card's Card Information Structure is interrogated *(see **061604.PDF**)*. If the CIS so indicates, the interface chip may be further programmed to change the card's power supply voltage, access timing, etc. Finally, the interface chip's address translation windows are set up to map the card's memory and I/O ports into the system address space, although the Databook chips can use either windows or their unique register-based interface. During normal operation, the interface chip's power management features—some automatic, some under software control—reduce power consumption during periods of card inactivity.

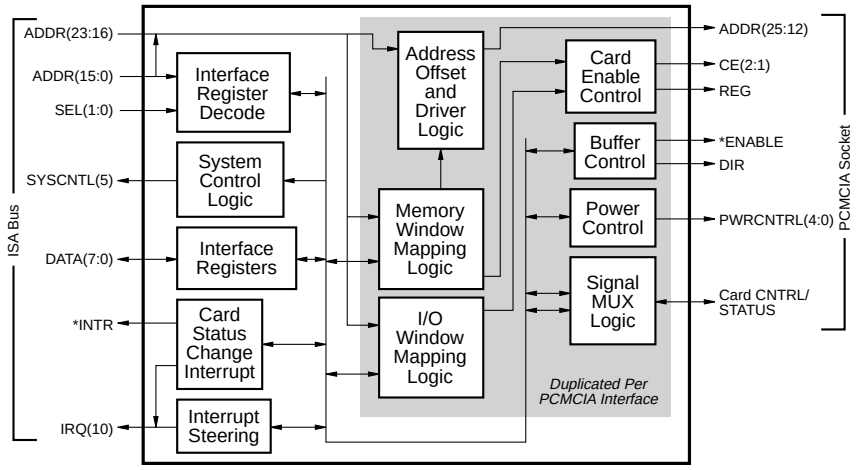

Figure 1. Block diagram of the Intel 82365SL. This chip provides no data buffering and only partial address buffering.

PCMCIA general features, ExCA influences both system software and the capabilities of PCMCIA interface hardware. Even though ExCA does not require it, the trend seems to be toward register-level compatibility with Intel's 82365SL PCMCIA interface chip.

Intel's 82365SL and Its Successors

The prototypical PCMCIA interface chip is Intel's 82365SL. It should be no surprise that the functions implemented on this chip support the Intel-defined ExCA architecture. While the other interface chips—except Databook's—are register-compatible with the 365SL, each has some extensions to the register set.

Register Offset	Register Name
00	Identification & Revision
01	Interface Status
02	Power & RESETDRV Control
03	Interrupt & General Control
04	Card Status Change
05	Card Status Change Interrupt Config.
06	Address Window Enable
07	I/O Control
08, 09, 0a, 0b	I/O Address Window 0 high & low
0c, 0d, 0e, 0f	I/O Address Window 1 high & low
10, 11, 12, 13	Memory Window 0 Map high & low
14, 15	Memory Window 0 Offset
18, 19, 1a, 1b	Memory Window 1 Map high & low
1c, 1d	Memory Window 1 Offset
20, 21, 22, 23	Memory Window 2 Map high & low
24, 25	Memory Window 2 Offset
28, 29, 2a, 2b	Memory Window 3 Map high & low
2c, 2d	Memory Window 3 Offset
30, 31, 32, 33	Memory Window 4 Map high & low
34, 35	Memory Window 4 Offset

Table 1. The 365SL implements 46 byte-wide, indirectly addressed registers per PCMCIA socket interface.

Thus, there are no exact 365SL clones.

There are currently two versions of the 365SL: the A-step and the B-step. Both versions are dual-socket controllers in 160-pin QFP packages. While the B-step is fully backward-compatible with the A-step silicon, it adds some new features, such as better power management. The B-stepping, which went into production in November, obsoletes the A-step silicon.

While a follow-on part that adds dual-voltage capability to Intel's line of PCMCIA interface chips is currently sampling, the other manufacturers already offer chips that can operate at either 5V or 3.3V. Due to a couple of register changes, Intel's 3.3V part will be almost (but not quite) backward-compatible with 365SL binary software. The 3.3V part will allow the ISA and PC Card interfaces to run on different voltages.

Figure 1 shows a block diagram of the 365SL. As the figure shows, each of the two PC Card interfaces has a dedicated copy of some hardware, such as the window-mapping logic. The buffer-control logic supports external buffers for the data bus and low address bits. The power-control logic simply drives pins that can be used to externally select voltages for Vcc, Vpp1, and Vpp2; no voltage-steering or -conversion logic is actually supplied on the chip.

Table 1 shows a summary of the 365SL's 46 internal one-byte registers. There are only two directly-addressable internal registers: the Index register and Data register, both one byte wide. All the registers listed in Table 1 are indirectly addressed by first writing the appropriate number into the Index register and then reading or writing the Data register. Register pairs that make up 16-bit logical registers, such as a window's low address limit, must be accessed one byte at a time.

The register set for controlling the first socket is accessed with the offsets given in Table 1, while the registers for the second socket are accessed by adding 0x40 to the offsets in Table 1. For a second 365SL, the registers are addressed at offsets 0xA0 and 0xC0.

For one or two chips, the directly-addressable Index and Data registers are accessed by the system CPU at I/O addresses 0x3e0 and 0x3e1, respectively. If a third or fourth 365SL are used, their Index and Data registers are at I/O addresses 0x3e2 and 0x3e3. To support more than four PCMCIA sockets with the 365SL requires some external address decoding.

The quad-register groups in Table 1 store high and low limit addresses in system space for each window. Since the memory windows are allocated in 4K chunks on 4K boundaries, these limit addresses are effectively shifted left by twelve bits. Similarly, the two registers for

each memory window offset store window offsets. Each offset—also shifted left by twelve bits—is added to the start and stop limit addresses to determine a window's location in the PC Card address space. This scheme, which is illustrated in Figure 2, allows access to the full PCMCIA address range, but only in segmented chunks.

In contrast to the memory windows, the I/O windows have single-byte granularity and are not offset from system space to PC Card space. The 16-bit I/O window limits allow I/O addresses to be mapped in the first 64K of system and card address space.

One of the advantages of PC Cards is that they allow end users to install peripherals without opening up their computer's enclosure, but since PCMCIA does not specify any mechanical interlocking, it is also be possible for a lazy user to insert or remove a PC Card while system power is fully active. This hot insertion and removal requires that all signals be fully isolated by buffers on a per-socket basis.

Due to pin limitations, the 365SL provides no buffering for data lines and only some address buffers. Thus, support for hot insertion and removal requires three extra jellybean glue chips per socket for full socket isolation.

As for power reduction, the A-step silicon provides essentially no support beyond turning off power to the socket. The B-step chip, on the other hand, reduces internal power consumption automatically when the memory and I/O windows are inactive. In addition, after software has set the power-down register bit and explicitly disabled the mapping windows and output buffers, power consumption can be further reduced by driving *CS high.

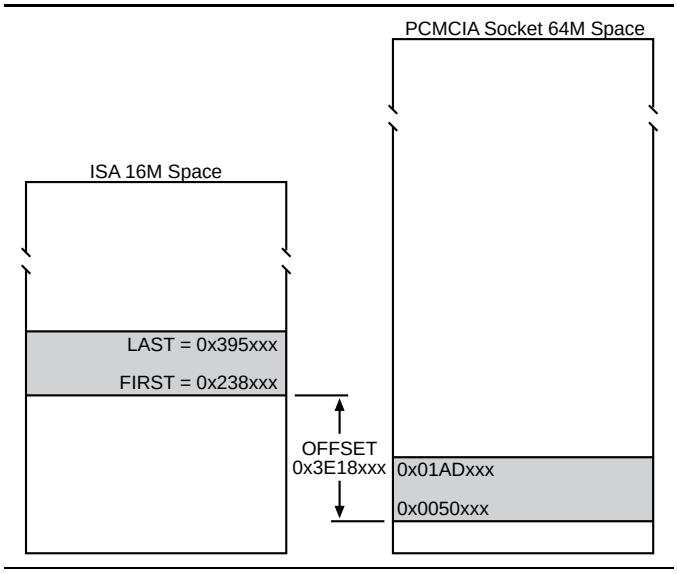

Figure 2. PCMCIA interface chips allow the 16M ISA address space to access all of the 64M PC Card address space through address windows. Each window specifies the high and low address limits in "FIRST" and "LAST" registers, and for memory windows, an OFFSET allows the address range to be translated from ISA to PC-Card space.

Cirrus 6710 and 6720

Cirrus Logic offers two versions of its PCMCIA interface chip: the single-socket, 144-pin VQFP ("very-thin") 6710 and the dual-socket, 208-pin QFP 6720. Both offer mixed-voltage operation, which allows the voltages for the PC Card interface(s) and the ISA bus interface to be independently operated at either 5V or 3.3V. This permits an additional degree of power savings.

The 67xx register set is a compatible superset of the 365SL. Like the 365SL, internal registers are accessed through index and data registers, but the 67xx allows both registers to be written with a single 16-bit access.

Fifteen additional registers control performance and function enhancements. Four of the extra registers implement two translation offsets for the I/O windows (I/O-window offsets are not present in the 365SL).

The 67xx chips provide flexible PCMCIA bus timing. The setup time (address and data stable before strobes), command-stable time (strobes are asserted), and recovery time (address and data stable after strobes) are independently programmable through three registers. Two sets of these registers allow two different timing profiles to be resident on the chip at once. Each I/O and memory window can be programmed to use either of the two sets of timing parameters.

To improve system performance when writing a string of values to a slow PC Card, the 67xx has a four-entry write FIFO; each entry is either a 16-bit word or a byte. As long as the FIFO has room, CPU writes to the chip complete with no wait states at ISA-bus speeds up

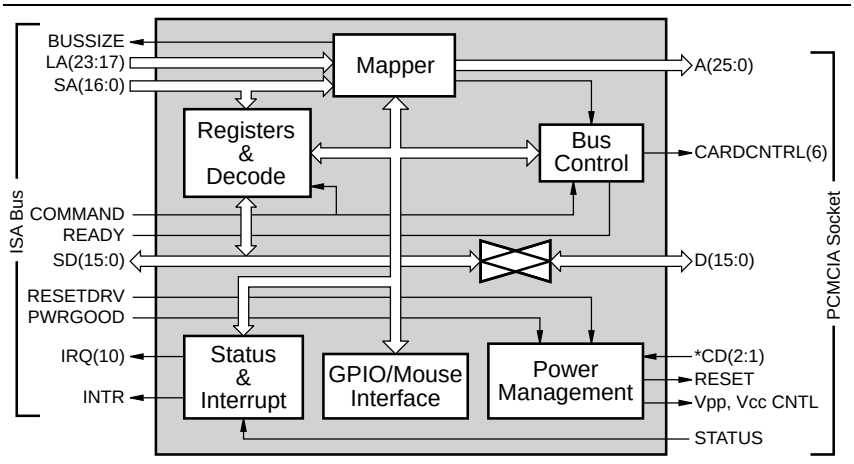

Figure 3. Block diagram of the Vadem 465. Note the full address and data buffering that allows hot-insertion/removal without external buffer chips.

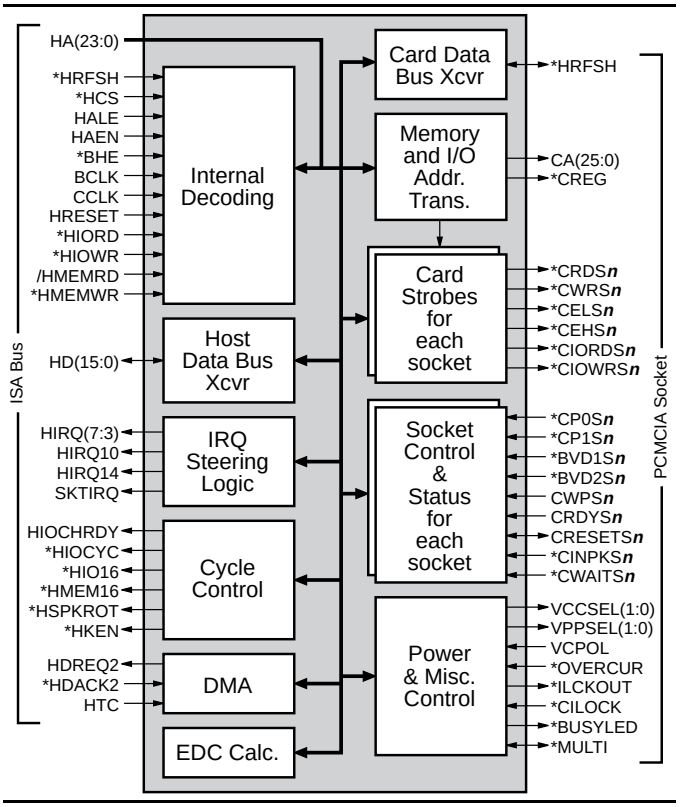

Figure 4. Block diagram of the Databook 86082. Hot insertion/removal is allowed as long as the user does not disturb a card while the busy LED is on.

to 10 MHz. If the FIFO has room, writes use the special two-cycle ISA "zero wait state" access instead of the normal three-cycle access.

A good application of the flexible timing and write buffer is changing a block of flash memory on a PCMCIA card. Flash programming software can be simplified by setting up timing parameters in a group of setup, command, and recovery registers and letting the chip's input FIFO buffer groups of bytes. Programming can be done in the background by bursting bytes into the FIFO during real-time-clock interrupts.

Another feature of the 67xx is its direct support for PCMCIA ATA-interface disk drives. "ATA" stands for "AT-Attachment" and is essentially the same as the IDE (Integrated Drive Electronics) interface. By setting a bit in a register, some of the PCMCIA pins are redefined according to the ATA definition.

The designers of the 67xx family chose higher-pin-count packages than Intel to allow on-chip implementation of hot-insertion buffers for data and address. This significantly reduces external chip count, but some external components are still required to control socket voltages.

Like the B-step 365SL, the 67xx chips have several power-saving modes. The automatic low-power mode is entered whenever the PCMCIA bus is inactive. It operates by stopping internal clock distribution and setting PCMCIA address and data lines to static values to prevent power dissipation in the input buffers of the PC Card. The 67xx suspend mode is easier to program than the 365SL's *CS powerdown; only a single bit in a register need be set. In suspend mode, all internal clocks are turned off and accesses to the sockets are ignored. The greatest power savings occur when the system addition-

About ExCA

The ExCA (Exchangeable Card Architecture) specification was written by Intel, and the current version is 1.10 dated June 12, 1992. This 62-page document defines an x86- and ISA-bus-specific PC-Card interface. The intent of the standard is to provide a design target that will guarantee interoperability between ExCA-compliant cards and systems. Something like ExCA was needed because the PCMCIA specification itself does not deal with some issues, such as the discrepancy between the sizes of ISA and PC Card address spaces.

An ExCA system has three distinct parts: hardware to control a PCMCIA socket; a low-level, socket-services software module; and a high-level, card-services software module. Socket services is written specifically for a given interface chip. Card services is, conceptually at least, independent of hardware (though still wedded to the x86 instruction set). Shortly after the ExCA specification effort began, Intel handed responsibility for card services over to the independent PCMCIA group.

The ExCA specification requires certain capabilities in the hardware, such as address-mapping windows, but otherwise uses socket and card services to isolate high-level software (operating systems and applications) from hardware particulars. The card and socket services provide a standard API (application programming interface) for interrogating and setting up PC Cards. Most applications will interact directly only with card services.

Intel is working to set up an independent test house for ExCA compliance certification. Though the test house will be independent, the test scripts will come from Intel, since Intel controls the ExCA definition. The first milestone is to have a DOS version of the compliance test available by March. In any case, the test will exercise only card- and socket-services calls and will not rely on 365SL-register-level compatibility.

Until a test suite is available, Intel will not comment on the ExCA compatibility of chips from any other vendor. Although testing is conducted on a chip/software combination, it will be interesting to see if vendors are forced to make changes in their chips to achieve ExCA certification. Software alone may not help Databook if the test suite attempts to activate all sockets simultaneously with five active memory windows each. On the other hand, if Databook can successfully lobby Intel, the tests may not exercise this corner case.

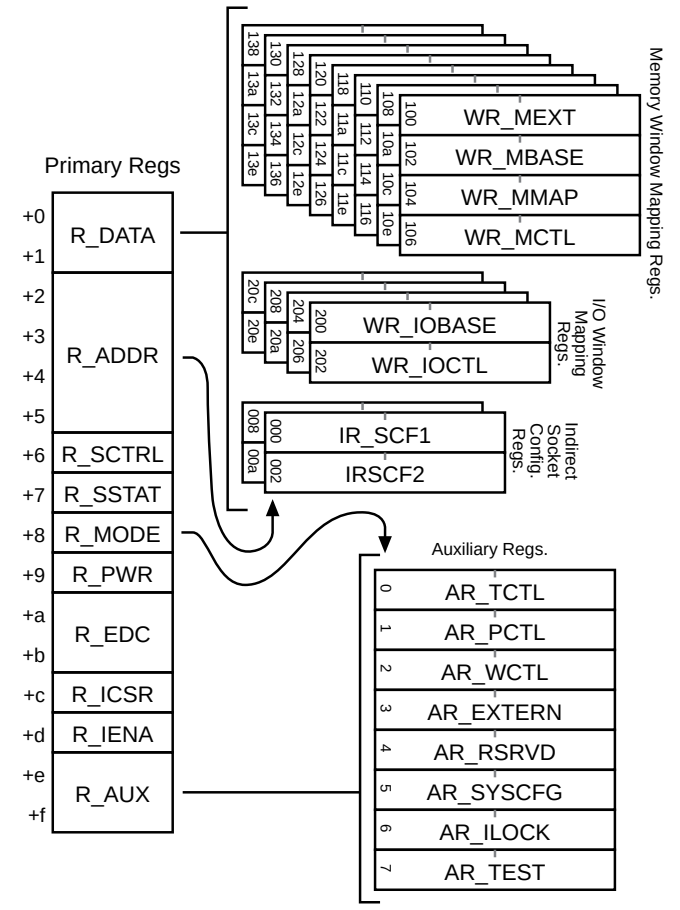

Figure 5. The Databook 86082 register set. The sixteen registers on the left are directly addressed through the ISA I/O space. The registers in the top group are accessed indirectly through R_DATA and R_ADDR. The auxiliary registers at the bottom are accessed indirectly through R_AUX and R_MODE.

ally sets the 67xx AEN signal high. This prevents ISA inputs from reaching core logic, which saves power by eliminating spurious internal core logic activity.

Vadem's VG465 & VG468

Like the Cirrus parts, Vadem's 465 is a register-compatible superset of the 365SL programming model. Currently, Vadem only offers a single-socket controller in its 144-pin 465, but the 208-pin, dual-socket 468 is currently in design.

Figure 3 shows a block diagram of the 465. While it can operate at either 5V or 3.3V, the 465 cannot operate its system and PC Card interfaces at different voltages like the Cirrus parts.

For hot insertion/removal, the 46x chips integrate full buffering like the Cirrus parts. In addition, the 46x implements the ExCA power-sequencing standard in hardware. ExCA power sequencing requires a time delay between the enabling/disabling of hot insertion buffers and application/removal of card power.

Price and Availability

The Intel 82365SL is available now in production quantities for less than $20 in 1000s. Intel, 3065 Bowers Ave., Santa Clara, CA 95051; 916/356-5262; fax 916/356-2692.

The Cirrus PD6710 is currently sampling; production pricing will be $21 in 1000s. The PD6720 will be sampling by the end of June; production pricing is expected to be $29 in 1000s. Cirrus Logic, 3100 West Warren Ave., Fremont, CA 94538; 510/623-8300.

The Vadem VG-465 is available now at $12.25 in 1000s; the VG-468 is currently in design. Vadem, 1885 Lundy Ave., San Jose, CA 95131; 408/943-9301; fax 408/943-9735.

The Databook 86082 is available now at $20 in 1000s. The Databook support software is also available now. Databook Inc., Tower Building, Terrace Hill, Ithaca, NY 14850; 607/277-4817; fax 607/273-8803.

Like the 365SL, multiple 46x chips can be cascaded for up to eight sockets using internal decoding. If a system needs more, an external chip select supports an unlimited number of sockets using external decoding logic.

The 465's eight superset registers offer a variety of features. One register controls an activity timeout counter that is retriggered by any card activity. When the timer expires, a status-change interrupt is generated to allow the system to put the chip into suspend mode. The timer interval can be one second to 15 minutes.

The 46x suspend mode is similar to that of the Cirrus parts: both are enabled by a single bit in a register. As with the other chips, suspend mode stops clocks and prevents PC Card access. In addition to software-enabled suspend, internal power consumption is reduced automatically when the address mapping windows are inactive.

Two superset registers control the functions of three general-purpose pins. These pins can be used to implement either a dedicated mouse port, one or two programmable chip selects, general inputs and outputs, or a variety of other miscellaneous functions. The base address and the block size of the chip selects are stored in three superset registers. Since the chip selects can be used for any address decoding purpose, they can save a PAL in some system designs.

The mouse logic has its own activity timer with a fixed duration of eight seconds. If eight seconds elapse without activity, the mouse interface goes into a low-power mode (clock stopped).

Like the 67xx family, the 465 also supports the PCMCIA ATA interface specification when a bit is set in its ATA superset register.

Databook's 86082

The Databook chip is the only PCMCIA socket controller that is not 365SL register compatible. However, it is still ExCA compliant since ExCA specifies a software architecture that can be supported by a variety of hardware organizations.

Figure 4 shows a block diagram of the 176-pin SQFP (shrink QFP) 86082, which is a dual-socket controller. Though it can operate from any voltage between 2.7V and 5.5V, the 86082 cannot accommodate different voltages on its ISA and PC Card interfaces.

No external buffers are required for hot insertion/removal so long as the end user heeds the busy LED, which indicates that one or both of the sockets is active. If hot insertion/removal is expected in an idle socket while the other socket is active, external buffers are required.

The busy LED is activated by the 86082, which detects card activity in hardware. Other chips have software-activated busy signals. Hardware activity detection is preferable when PCMCIA cards are emulating standard motherboard peripherals, since no PCMCIA or ExCA software layers are involved in this case.

The 86082 implements 112 internal one-byte registers, but most are grouped to form 16-bit logical registers. As shown in Figure 5, sixteen are directly addressable through the default I/O addresses of 0x240 through 0x24f. External address decoding for these registers is possible if a different address range is required.

Most of the indirect registers are addressed by placing an index value in the R_ADDR register quadruple and then accessing R_DATA. The auxiliary registers are accessed by writing an index into R_MODE and then accessing R_AUX. R_ADDR and R_DATA can also be used to access the PC Card address space, which gives driver and application software a way to directly address PC Cards without using the window scheme.

In contrast to the 365SL-compatible mechanism, the 86082 allows its registers to be accessed two bytes at a time, which improves performance. In addition, addressing most of the indirect registers can be done with a special auto-increment addressing mode that improves performance by eliminating the overhead of rewriting a new index into R_ADDR when groups of contiguous registers are written, such as when initializing memory-mapping windows.

The ExCA specification calls for five memory and two I/O mapping windows per PCMCIA socket. In the Intel-compatible implementations, this requirement led to windows dedicated on a per-socket basis. The 86082, on the other hand, implements a total of eight memory and four I/O windows; each can be assigned to either socket.

It remains to be seen if the lack of the fifth memory window present in the 365-compatible designs presents a compatibility problem. Databook claims that the direct, register-based interface through R_ADDR and R_DATA makes up for the lack of the fifth window. While the 86082 would seem to be incompatible with an application that requires five simultaneous memory windows, Databook says this situation never occurs in practice. Databook points to its large number of design wins as proof of its ExCA compatibility.

One unique feature of the 86082 is its EDC (error detection) unit. This unit can be programmed to accumulate either a one-byte checksum or a 16-bit CRC of all data that is transferred explicitly by software through the R_DATA port. Since the data for normal card accesses flows around the chip, only software routines that explicitly write an address to R_ADDR and then access R_DATA can take advantage of the EDC unit. The Databook socket services software, however, makes use of the R_DATA port instead of windows as often as possible. The EDC function is particularly useful for disk-like, serial access patterns where auto-incrementing and checksum accumulation can be done on the fly to increase performance.

Another unique feature is the support for DMA. Although the PCMCIA specification does not call for DMA support, the 86082 provides it using what PCMCIA terms a "custom interface." DMA can be used to support a PC Card interface to a PC/AT-compatible external floppy disk.

The 86082 has a set of timing generators to aid in writing to non-volatile memories and in generating wait states for slow system buses. There are two eight-bit counters that are intended to support the 6-µs and 10-µs critical programming times of the most popular devices. With these hardware timers, software loops are unnecessary, leaving the main CPU free for other tasks.

Although there is no explicit, software-enabled power-saving mode as with the other chips, the 86082 has an automatic mode that achieves similar effects. Two clock cycles after the 86082 is deselected, internal clocks are stopped and input buffers are disabled.

Evaluation and Conclusions

The current crop of PCMCIA interface chips offers a fairly wide range of choices. To Intel's delight, ExCA appears to be firmly entrenched as the standard for PCMCIA on x86-based platforms, and vendors appear to be mostly towing the line of 365SL register-level compatibility. Databook is the single holdout, and while their contention that ExCA compliance does not require register compatibility with the 365SL is true, it may be moot if system makers and BIOS vendors demand 365SL look-alike parts.

One question is just what register-level compatibility will mean in the future. Even the non-Intel-compatible parts have unique extensions, and Intel's 3.3V part is not 100% compatible. BIOS and driver software can hide

register-level differences, but it remains to be seen if a least-common-denominator, de facto standard will emerge.

Intel's parts do not have an explicit ATA disk-interface mode, which is a deficiency according to some vendors. Intel maintains that its testing shows the 365SL capable of handling all available drives with the notable exception of HP's 1.3" KittyHawk drives.

For the smallest portable devices, a single PCMCIA slot is probably sufficient, and it is likely that the socket interface will be integrated into the CPU or chip set. This has already been done on C&T's PC/Chip.

Pin limitations, however, will make discrete controller chips more practical for two or more sockets, and semiconductor vendors with successful chips can look forward to a growing market. An ISA-bus interface may be only an interim trend; PCI or other local bus interfaces probably make more sense in the long term.

PCMCIA slots make just as much sense for desktop machines as for portable devices. Chip-set vendors are likely to offer PCMCIA interface chips as part of their chip sets, but they can probably add little value compared to the existing chips. Pin-count limitations suggest that full integration of PCMCIA interfaces into an existing chip set will be limited to a single socket.

Since these chips are architecturally simple and a really practical PCMCIA socket interface requires the ability to gate either 5V or 3.3V to an installed PC Card, there appears to be an opportunity for mixed analog/digital technology. A truly single-chip PCMCIA controller would have the ability to do the voltage gating internally, and there are rumors that such chips are being developed.

Although these chips are functionally simple, there are many subtleties. If performance for a certain application area is important, perhaps the write FIFO of the Cirrus parts or the auto-increment capability of the Databook part are compelling. If true hot insertion/removal capability with minimum chip count is critical, the Cirrus or Vadem parts are a good choice.

Even the chips that are register-set compatible with the 365SL have significant differences. ExCA compatibility is a clearly established requirement, but it does not necessarily imply 365SL register-level compatibility. While it seems safest to use a 365SL-compatible chip, Databook's claim of a large number of design wins implies that they have successfully addressed the issues with their own software. The Intel parts have the least-developed feature set, but may offer the best prospects for future compatibility since Intel controls the ExCA standard. ♦

