Intel Unveils First PCI Chip Set

Three-Chip Set Supports High-End 486 ISA Systems

By Michael Slater

Comdex demonstrations of the first silicon supporting Intel's Peripheral Chip Interconnect (PCI) bus marked the start of the most radical change in the PC architecture since its inception. Intel showed the first PCI system-logic chip set, the 82420, working with the first PCI peripheral chip—NCR's 53C810 SCSI controller. While no other PCI products were shown, several graphics controller, system-logic, and other silicon vendors announced plans to support PCI. Even Intel's arch-rival AMD expressed strong interest in PCI.

PCI is an intermediate bus that is intended to serve as the central interconnect for system logic and high-performance peripherals *(see **060902.PDF**)*. It is a multiplexed, 32-bit bus with a 33-MHz maximum frequency. It supports variable-length burst reads and writes, and a 64-bit extension has been defined. PCI is designed to serve both as a chip-level interconnect for peripherals that are on the motherboard and as a bus for high-performance expansion cards, although the expansion connector has only recently been defined and is still not officially approved.

PCI is often compared to VESA's VL-Bus, and both are designed to meet many of the same goals. (PCI is also conceptually similar to Sun's SBus and DEC's TurboChannel, but these buses do not compete directly because they are associated with different platforms.) VL-Bus motherboards from about a dozen vendors were shown at Comdex, and virtually every major graphics board or chip maker is supporting it. VL-Bus is here now, and it will be widespread in high-performance PCs for at least the next year or two. PCI, however, has the support of the industry's heavyweights (see sidebar). While PCI will not be as significant as VL-Bus in 1993, it will be far more important in the future.

Intel's Chip Set

Intel's 82420 chip set is designed for high-end, performance-oriented PCs—what Intel calls business workstations, or professional business PCs. Typical systems are expected to sell in the $2500–$3500 range. The initial version supports the ISA bus, and an EISA version will follow early next year. A lower-cost version, designed for mainstream "value" PCs, is planned for the second half of 1993. The lower-cost version is likely to find applications in portable systems as well.

Figure 1 shows a block diagram for a PCI system based on Intel's new chip set. There are three chips in the set: the 82424TX Cache/DRAM Controller (CDC), the 82423TX Data Path Unit (DPU), and the 82378IB System I/O (SIO). The CDC and SIO are in 208-pin QFP packages, while the DPU is in a 160-pin QFP.

The CDC is the heart of the chip set. It interfaces the 486 bus to the PCI bus, and it includes a second-level cache controller and a DRAM controller. It works in conjunction with the DPU, which provides the data-path logic; pin-count limitations on low-cost packages prevent these two devices from being combined into one.

The memory controller is designed for use with 70 ns fast-page-mode DRAMs. It provides a 3-1-2-1 access pattern (i.e., the first access of a burst takes 3 cycles, the next takes 1 cycle, etc.) for 25-MHz systems, 4-1-2-1 at 33 MHz, or 6-2-4-2 at 50 MHz. Memory sizes from 2M to 128M are

PCI Supporters

AMD, ATI, Adaptec, and National were elected to the PCI Steering Committee in a meeting at Comdex, joining founding members Intel, IBM, Compaq, DEC, and NCR. Other system makers that have joined the PCI special interest group include Acer, AST, Dell, Epson, HP, Hitachi, NEC, Oki, Olivetti, Siemens, Tandy, Toshiba, Unisys, and Zenith. If even half of these system vendors actually produce PCI systems it will be a very important standard.

Several other chip-set vendors have committed to developing PCI system-logic chips. VLSI plans to sample a 486 chip set in 1Q93, a Pentium chip set in 2Q93, and a laptop version at some later date. LSI Logic also expects to sample a Pentium chip set in 2Q93. Western Digital plans to develop a 486 chip set but has not released any timeframe.

So far, no PCI graphics chips have been demonstrated. Intel used external glue logic to adapt ATI's Mach32 controller to the PCI bus for its Comdex demonstrations. ATI has announced plans to sample a PCI version of its 68800 graphics controller in January. Weitek showed its Power 9000 graphics chip interfaced to Intel's PCI chip set, and Weitek plans to introduce a PCI version of the chip in 1Q93. Avance Logic has promised a PCI graphics chip by the end of this year. Others who have promised to have samples in 1Q93 include Cirrus Logic, Matrox, NCR, S3, and Tseng Labs. Chips and Technologies, VLSI Technology, and Western Digital all plan to introduce PCI graphics chips later in 1993.

NCR is not the only company planning a PCI SCSI chip. TMC plans to have a SCSI controller in 1Q93, and Adaptec, Future Domain, and Western Digital all plan to follow later in the year.

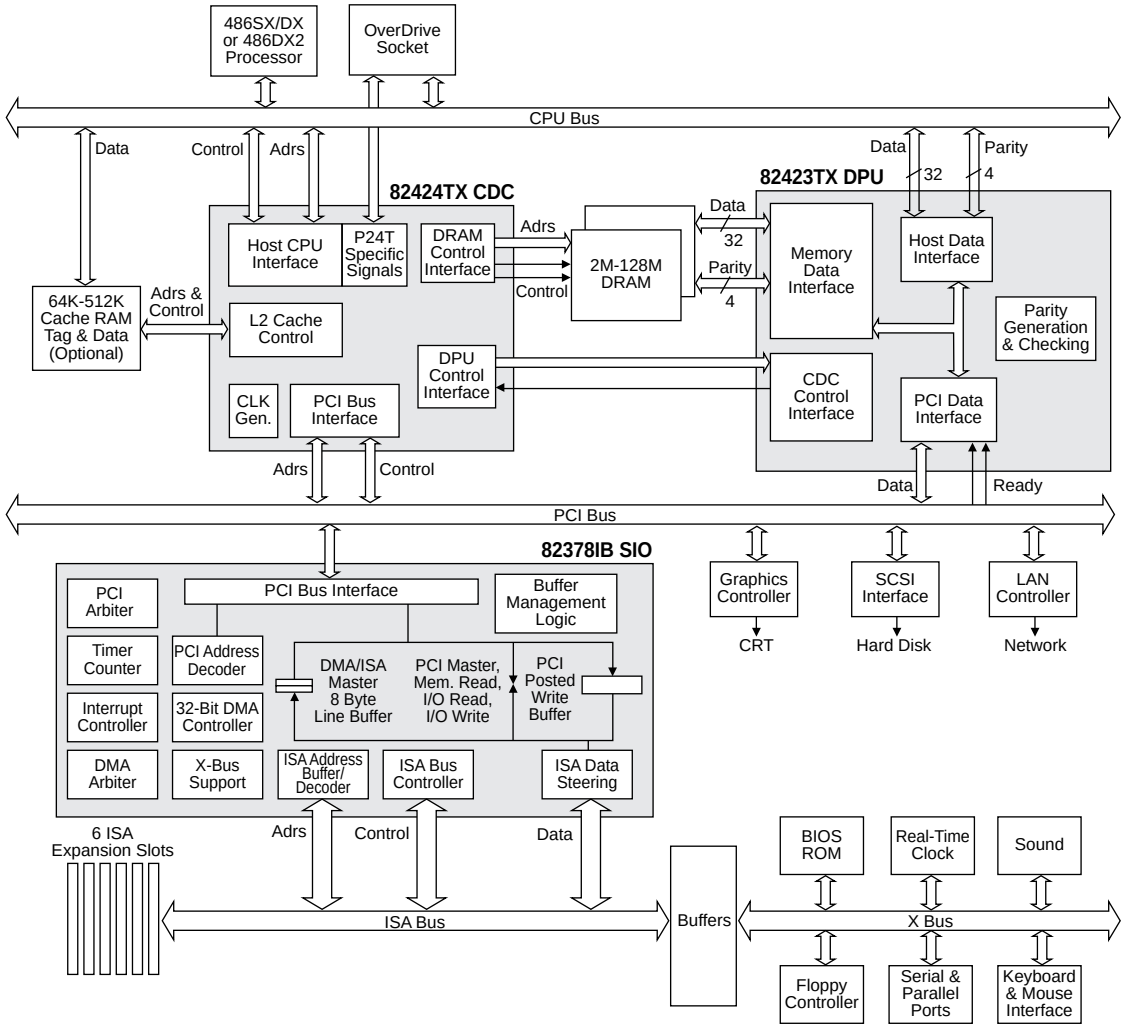

Figure 1. Block diagram of a PCI system using Intel's 82420 chip set.

supported using 256K × 4, 1M × 4, and 4M × 4 DRAMs. The DRAM is two-way interleaved.

The second-level cache controller offers both write-through and write-back modes. External SRAMs are used for both data and tags. Cache sizes supported are 64K, 128K, 256K, and 512K. Using common 32K × 8 SRAMs, the minimum cache size is 128K. In addition to four byte-wide SRAMs for the main cache array, another 8- or 9-bit-wide SRAM is required for the tags. With an 8-bit-wide RAM for the tags and a 128K cache, the maximum cacheable memory is 32M; using a 9-bit-wide RAM for the tags doubles the maximum cacheable memory to 64M. For 33-MHz operation, the access times required are 20 ns for the data SRAMs and 12 ns for the tag SRAM. At 25 MHz or 50 MHz, these times are relaxed to 25 ns and 15 ns, respectively. As in most 50-MHz PC designs, cache accesses require two cycles at this clock rate.

Full hardware cache coherency support is provided; in write-back mode, the cache snoops on both read and write cycles performed by other PCI masters. On a read snoop hit, the PCI transaction is stalled, the dirty data from the cache is written to main memory, and the PCI transaction is then allowed to continue. The chip set does not support multiple processors on the PCI bus, although non-cached masters (such as a graphics or LAN controller) are allowed. Coherency with the first-level cache is maintained by snooping both the processor's on-chip cache and the second-level cache; inclusion is not used.

The CDC supports the forthcoming "OverDrive processor for 486DX2 systems," code-named the P24T, which is an end-user upgrade version of the Pentium

Price & Availability

Samples of the 82420 chip set are available now for 25- and 33-MHz operation. The production version of the silicon will support 50-MHz operation and scatter/gather DMA; samples of this version are planned for March '93, with production in April. In quantities of 10,000, the chip set is priced at $52.80 for all clock frequencies. For additional information, contact your local Intel sales office or call 800/548-4725 and ask for literature packet #HP-58.

Copies of the PCI specification are available from the PCI Special Interest Group for $100 each. Companies planning to build PCI products can join the PCI SIG for $2500, which includes updates to the specification, technical support, and the opportunity to submit proposals for future revisions. Contact the PCI SIG at 503/696-2000.

First PCI Peripheral

NCR's 53C810 SCSI controller is the first PCI peripheral chip to be demonstrated. The 53C810, based on NCR's established 53C700-family devices, operates as a PCI bus master. NCR's SCSI Device Management System software, based on ANSI's Common Access Method (CAM), simplifies the software task of supporting a variety of SCSI peripherals.

The 53C810 supports asynchronous SCSI transfers at up to 5 Mbytes/s and synchronous transfers at up to 10 Mbytes/s. The chip includes a 64-byte DMA FIFO and an 8-byte synchronous SCSI FIFO. It is compatible with NCR's SCRIPTS programming language for SCSI command sequencing.

The 53C810, which is packaged in a 100-pin PQFP, is priced at $32.40 in thousands. Small quantities will be available in 1Q93, with volume production in the second quarter. Contact NCR at 800/334-5454 or 719/596-5795.

processor. This chip will plug into the extended OverDrive socket that includes extra signals to support the processor's on-chip write-back cache. Cyrix's recently announced 486S2/50 *(see **0615MSB.PDF**)* and its forthcoming M7 processors both provide write-back caches using a similar protocol. While this was surely not Intel's intent, the P24T support signals in the CDC are likely to also be adaptable for use with the Cyrix devices.

The DPU provides three separate 32-bit data paths: one each for the processor, DRAM, and PCI bus. Several FIFO buffers isolate the buses. Separate four-level FIFOs handle CPU-to-memory and CPU-to-PCI transactions, a two-level FIFO buffers PCI writes to the memory, and another two-level FIFO stores data prefetched from DRAM for either the CPU or a PCI master. The CPU-to-memory buffer also serves as a holding register for dirty cache lines when a line must be flushed; it stores a dirty line waiting to be written while read requests are processed to refill the cache line.

The PCI bus supports burst reads and writes, but the 486 processor uses only burst reads. Display memory accesses, however, are predominantly writes, and they typically occur in sequential bursts, making them a perfect candidate for burst writes. The CDC and DPU combine sequential writes from the processor into burst writes on the PCI bus. The CDC includes an address FIFO that tracks the entries in the DPU's processor-to-PCI data FIFO. When the buffer includes two or more entries with sequential addresses, a burst transfer is performed. The chip set will continue bursting as long as there is another item in the FIFO with a sequential address. The FIFOs do not implement byte gathering, so bursting works only for 32-bit accesses.

Intel claims that the data buffering and burst support provide a significant performance increase over direct local-bus implementations. When a graphics controller is connected directly to the processor's local bus, wait states are generally required for write cycles. With the PCI chip set, write cycles from the processor are completed without wait states (as long as there is room in the DPU's FIFO), and the writes can then be bursted to the PCI graphics controller while the processor continues with other operations. Intel believes that this will provide a performance boost of at least 10% over other local-bus implementations. (Although a similar buffering and burst transfer scheme could be implemented for the VL-Bus, existing VL-Bus implementations do not isolate the processor bus in this way.)

I/O Controller

The third device in Intel's 82420 PCI chip set is the System I/O (SIO) chip, which interfaces the PCI bus to the ISA bus and provides the PC-standard interrupt controller, DMA controller, and timer/counters. This chip also includes the PCI bus arbiter, which supports up to two PCI masters in addition to the CDC and the SIO itself, and support logic for the 8-bit X-bus used for low-speed peripherals.

The SIO's DMA controller is borrowed from Intel's EISA chip set. In addition to standard ISA DMA transfers, which require 8 BCLK (bus clock) cycles each, it also supports EISA's "type A" (6-cycle) and "type B" (4-cycle) modes. Going one step further, the SIO's DMA controller adds a new type, called "F" or "fast," which uses only 3 clock cycles per transfer for a peak data rate of 5 Mbytes/s. Most recent peripheral chips can handle the A, B, or F cycle types. Western Digital's "Caviar" IDE disk drives support type F DMA transfers.

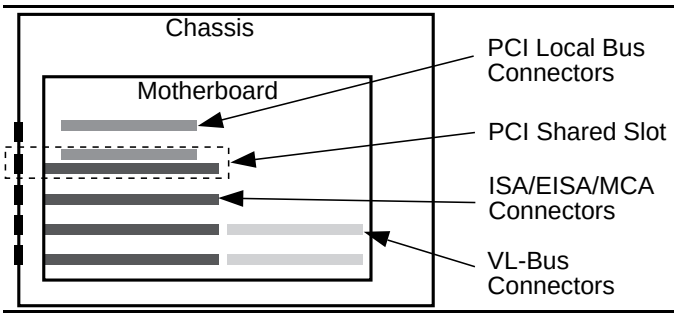

Figure 2. PCI and VL-Bus connector placement.

Another improvement in the SIO's DMA controller is support for 32-bit linear addressing (as in EISA), in addition to the clumsy, segmented approach dictated by ISA. Intel plans to go even further in the production version of the SIO chip by adding scatter/gather capability. All the advanced features are optional; by default, the DMA controller is ISA-compatible. The fast transfers, linear addressing, and scatter/gather modes must be enabled by driver software customized for the chip set.

Future Versions

To support other expansion buses only the SIO chip needs to be changed. Intel plans to have a two-chip EISA version of the SIO device in the first quarter of 1993. Because of the anemic state of the Micro Channel market (outside of IBM's own systems), no Micro Channel version is currently planned. IBM or one of the makers of Micro Channel compatible machines could, however, develop its own SIO chip for use with Intel's CDC and DPU, which would be much simpler than developing a complete PCI/Micro Channel chip set.

Similarly, different processors can be supported by replacing the CDC and DPU chips. Intel plans to have a Pentium version of the chip set ready to ship along with the Pentium processor late in 1Q93; this version will have a new CDC and DPU, and it will presumably support a 64-bit-wide memory system.

DEC has announced that it plans to use PCI for future Alpha-based PCs. DEC plans to integrate the PCI interface on its low-cost Alpha chip, eliminating the need for the CDC and DPU devices. By using PCI, DEC can tap into expansion bus interface chips (such as Intel's SIO), graphics, LAN, and SCSI controllers being developed for the bus, allowing the relatively low-volume Alpha systems to benefit from chips developed for the high-volume PC market. An R4000-to-PCI chip set also seems inevitable, although no specific plans have been announced. Eventually, an R4000 derivative with a direct PCI interface seems likely to appear.

PCI Connector Proposed

One weakness of PCI as originally defined last June is that no connector was specified, limiting its applicability to motherboard designs and proprietary connectors. The PCI special interest group has now proposed a connector definition, which was presented to the committee meeting at Comdex and is expected to be officially sanctioned by the end of the year.

The PCI group selected the same connector as VESA's VL-Bus: the 16-bit Micro Channel connector, a card-edge type with 0.1" contact spacing. As Figure 2 shows, the proposed PCI standard puts the PCI connector adjacent to a standard ISA, EISA, or Micro Channel connector. The VL-Bus standard, on the other hand, places its connector in line with the standard expansion bus connector.

The PCI approach has the advantage of allowing half-size add-in cards and using less motherboard real estate. The VL-Bus approach has its own advantages; it makes signal routing much easier and allows add-in cards to connect to both the VL-Bus and the standard expansion bus.

PCI vs. VL-Bus

Today, if you want to buy a PC with a standard local bus, VL-Bus is the only choice. Dozens of VL-Bus motherboards, system-logic chip sets, peripheral chips, and add-in boards are now available, and many more will ship in the next few months. The VL-Bus effort has a head start largely because it is easier to implement; it is a simple extension to the 486 bus, and existing chip sets and peripheral chips are easily adapted.

PCI, on the other hand, requires more radical changes to silicon designs, but it will have a more profound impact on system architecture. For the next year or so, VL-Bus systems will be widespread, while PCI systems will be rare and relatively expensive. PCI add-in cards will be even rarer.

It is possible (though more expensive) to build a PCI system with VL-Bus slots—or even with both VL-Bus and PCI slots—for add-in boards. If the range of VL-Bus add-in boards is sufficiently compelling, some systems using this approach may emerge. Despite this possible scenario for coexistence, however, PCI is likely to obsolete VL-Bus in the long term.

While PCI has some potential technical advantages (such as the use of a multiplexed bus, which reduces pin count, and auto-configuration, which simplifies user installation of add-in boards), its key advantage is the backing of Intel and many of the industry's major OEMs. The PCI market will grow slowly at first, starting with high-end systems. Once system-logic chip sets are available at various price/performance points from several vendors and a variety of peripheral chips is available, it will quickly grow to play a major role across the PC spectrum. Ultimately, processors with direct PCI interfaces will propel the standard to dominance, possibly in some RISC-based systems as well as x86 systems. ♦

