Literature Watch

Buses

Buscon reveals the latest serial-line technology. *Serial-bus issues make their mark at Buscon 92 East.* Richard Nass, Electronic Design, 9/17/92, pg 57, 5 pgs.

Increasing sales and instrument availability herald onslaught of a real VXI revolution. Michael L. Porter, Pers. Eng. & Inst. News, 10/92, pg 31, 8 pgs.

First Futurebus+-to-VME bridge board appears. Warren Andrews, Computer Design, 10/92, pg 30, 3 pgs.

Development Tools

System simulators meet wireless challenges. *Designers of wireless RF and microwave systems can turn to specialized software tools to help them simulate complex systems efficiently.* Doug Conner, EDN, 9/17/92, pg 39, 7 pgs.

Performance analysis spots hardware/software bottlenecks. Tom Williams, Computer Design, 10/92, pg 61, 6 pgs.

DSPs

Special tools, techniques uncover tough problems in mixed analog/digital systems. Dick Benson, Tektronix Inc.; Pers. Eng. & Inst. News, 10/92, pg 49, 6 pgs.

EDN's DSP-chip directory. David Shear, EDN, 9/17/92, pg 90, 28 pgs.

Graphics

The virtues of the hue, lightness, saturation color model. *If you thought RGB (red, green, blue) was the only (or best) way to represent color, think again. The hue, lightness, saturation (HLS) model can actually be better than RGB at representing colors in some applications.* James R. Furlong, The Computer Applications Journal, 10-11/92, pg 50, 8 pgs.

Memory

Specialty PROMs count bursts, implement state machines. Don Tuite, Computer Design, 10/92, pg 52, 3 pgs.

Special report—high speed DRAMs. *Memory catches up; Fast computer memories; Fast DRAMs for sharper TV; A new era of fast dynamic RAMs; A fast path to one memory; A RAM link for high speed; Fast interfaces for DRAMs.*, IEEE Spectrum, 10/92, pg 34, 22 pgs.

Miscellaneous

Design and implementation of a multi-microprocessor architecture for image processing. Arun Vaidyanathan, Cirrus Logic Inc., Eric M. Dowling and Poras T. Balsara, University of Texas at Dallas and Erik Jonson School of Engineering; Microprocessors and Microsystems, v16 #6-92, pg 321, 10 pgs.

Is neural computing the key to artificial intelligence? Mike Donlin, and Jeffrey Child, Computer Design, 10/92, pg 87, 14 pgs.

The V.42bis standard for data-compressing modems. Clark Thomborson, University of Minnesota at Duluth; IEEE Micro, 10/92, pg 41, 13 pgs.

Superconductivity moves from the land of theory into the land of reality. *The successful development of reliable, compatible, low-cost superconducting circuits could benefit every application involving microelectronics and ICs.* Tom Ormond, EDN, 10/1/92, pg 49, 5 pgs.

Peripheral Chips

Networked controllers talk over power lines. *Enhanced spread-spectrum technique pushes control-network communications through powerline clatter.* Milt Leonard, Electronic Design, 9/17/92, pg 73, 4 pgs.

High-speed A-D converters shift to new architectures. Jeffrey Child, Computer Design, 10/92, pg 129, 5 pgs.

Programable vision processor/controller for flexible implementation of current and future image compression standards. Doug Bailey, Matthew Cressa, Jan Fandrianto, Doug Neubauer, Hedley K.J. Rainnie, and Chi-Shin Wang, Integrated Information Technology; IEEE Micro, 10/92, pg 33, 7 pgs.

Programmable Logic

The best aspects of PLD- and FPGA-based design revolve around device partitioners. Russ Lindgren, Pers. Eng. & Inst. News, 10/92, pg 39, 10 pgs.

FPGA advances cut delays, add flexibility. *Improved FPGA architectures and processes increase gate counts, speed, and open new applications.* Dave Bursky, Electronic Design, 10/1/92, pg 35, 5 pgs.

RAM-based logic arrays up density, cut delays. *Combination coarse-grain/fine-grain logic arrays offer up to 24,000 usable gates and the best performance of any alterable array.* Dave Bursky, Electronic Design, 10/1/92, pg 45, 4 pgs.

Choosing complex PLDs and FPGAs. Anne Watson Swager, EDN, 9/17/92, pg 74, 10 pgs.

SRAM-based FPGAs offer predictable timing, cascadable counter sections. *Field-programmable gate arrays join the company's EPLD families, all using the same design software.* Electronic Products, 10/92, pg 75, 2 pgs.

System Design

Flexible I/O subsystem gives MCU many resources. *A programmable I/O subsystem lets a 16-bit microcontroller provide multiple peripheral functions without recasting the silicon.* Dave Bursky, Electronic Design, 10/15/92, pg 53, 5 pgs.

Massively parallel system delivers 68,500 MIPS. *Holding up to 16 boards and 16,384 processors, a board-level system outperforms larger and more expensive mainframe conputers.* Richard Nass, Electronic Design, 10/15/92, pg 89, 2 pgs.

PC power management. *In recent years, the portable computer has spawned an outbreak of innovations to conserve battery power.* John Gallant, EDN, 10/15/92, pg 115, 6 pgs.

