IDT R3041 Lowers Embedded MIPS Entry Cost

Cost-Reduced R3051 Aimed At Low-Cost Laser Printers

By Brian Case

IDT's R3041, its latest MIPS-architecture microprocessor for embedded control applications, brings the MIPS architecture down to lower price points than ever before—$15 in volume for a complete CPU with on-chip cache. To reduce microprocessor cost, it has much smaller caches than IDT's earlier models, the R3051, R3052, and R3081. To reduce system cost, it has a counter/timer for DRAM refresh and new bus control flexibility that allows a system to mix memories and devices of different widths. The R3041 fits in with the current family members by sticking with the existing 84-pin package and implementing a signal superset that allows systems to be upgraded by changing only the microprocessor.

Chip Overview

As shown in Figure 1, the basic organization of the R3041 is the same as its higher-performance siblings. The R3000-derived CPU core gives it the same basic integer execution capabilities, except that the MMU has been removed. The major differences are the smaller caches, the timer/counter, and the data packing and unpacking capability in the bus controller.

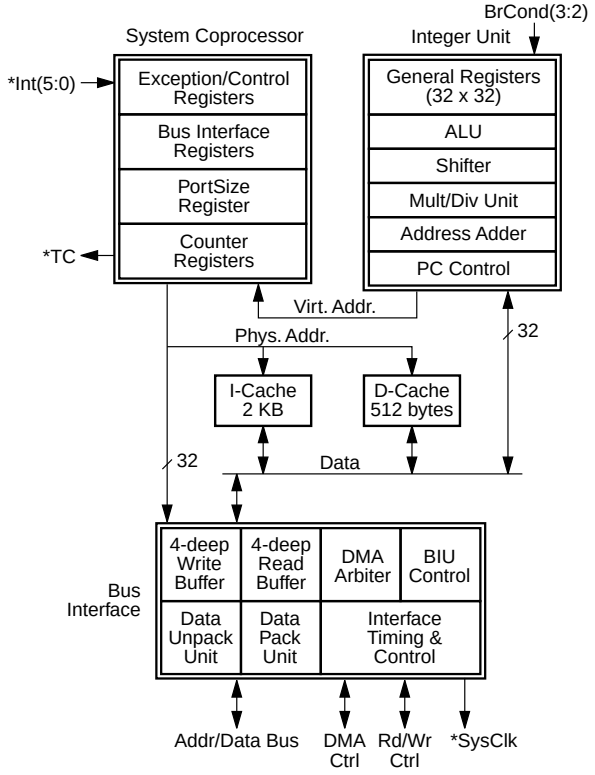

Figure 1. Block diagram of the R3041.

The on-chip caches are small—2K for instructions and 512 bytes for data. The R3051 caches are four times larger, while the R3081 has caches eight times as big. Some of the important existing low-cost embedded controllers have no cache at all, which means the R3041 will have a performance advantage for a given clock rate on applications that exhibit good cache behavior. The I-cache has a line size of four words while the data cache has a one-word line size.

The timer counter facility consists of two registers: a 24-bit up-counter and a 24-bit compare register. When the value in the count register equals the compare register, the *TC output is asserted and the count register is cleared. *TC can be connected externally to one of the interrupt input pins or used to implement DRAM refresh. A bit in BUSCTRL (system coprocessor register 2) determines whether *TC is reset either automatically (for DRAM refresh) or by software.

Bus Controller Enhancements

Two system control registers control the new features that support mixed-width memories: PORTSIZE and BUSCTRL. PORTSIZE has a two-bit field for each of fourteen sub-regions of the physical address space. Each two-bit control field determines whether the bus controller treats the memory in the corresponding physical address range as 8-, 16-, or 32-bit memory. This capability is very similar to that of AMDs 29200, and IDT's justification is much the same as AMD's: It is advantageous to be able to support 32-bit DRAM and an 8-bit boot PROM with the option of 16-bit laser-printer font cartridges.

The BUSCTRL register has fields that allow the two coprocessor-condition inputs to become outputs that fine-

Price & Availability

The R3041 will be packaged in an 84-pin PLCC and offered in 16- and 20-MHz versions. Samples will be available by the end of the year with production scheduled for the first quarter of 1993. In 1000s, the 16-MHz and 20-MHz versions will be $24 and $30, respectively. Prices drop to $15 and $19 for orders of 50K.

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tune the timing of some of the bus control signals. The two BrCond inputs become outputs (*ExtDataEn and *IOStrobe) that have more relaxed timing than standard R3051 bus signals, which allows a buffer-less interface to relatively slow devices and memories.

In addition to the four byte-enable signals (BE[3:0]) for the standard 32-bit interface, the R3041 implements two additional byte enables (BE16[1:0]) for use by 16-bit memory blocks. A mode is available that allows the BE signals to be connected directly to the write-enable signals of DRAM chips.

Performance

The R3041 compares more or less favorably to the R3051 depending on the benchmark suite used. For the Intel Standard Integer Benchmarks, which are quite small, the R3041 performance averages about 15% less than the R3051. On an IDT suite of 18 different real applications (oriented to page description languages such as PostScript), the average is 15 to 35% less. IDT claims that a 16-MHz, 16-bit-bus R3041 is close to twice the performance of a 20-MHz, 32-bit-bus 960KA on the Intel benchmarks.

Conclusions

IDT is eyeing the embedded markets that AMD and Intel have cultivated: low-cost, moderate-performance laser printers and X-terminals. Compared to the 29200, the R3041 has equal ability to accommodate a mixed-width memory system and probably offers measurably higher performance. The 29200, however, still offers slightly better system integration with its video interface and on-chip DRAM control.

The most compelling features of the R3041 are its caches, which can enhance performance, and its aggressive price. The R3041 is a sensible evolutionary step for IDT since the chip meets the needs of important market segments with features that are not overly specific. ♦

